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It is respectfully submitted that the transitional phrase "consisting essentially of" is not exclusionary and does not provide a negative limitation. While M.P.E.P. § 2111.03 defines the phrase "consisting of" as an exclusionary phrase, that same section indicates that the phrase "consisting essentially of" merely "limits the scope of a claim to the specified materials or steps 'and those that do not materially affect the basic and novel characteristic(s)' of the claimed invention. *In re Herz,* 537 F.2d 549, 551-52, 190 USPQ 461, 463 (CCPA 1976) (emphasis in original) . . ."

Moreover, it is respectfully submitted basis for the recitation of "consisting essentially of" in claims 1 and 20 is provided by the specification of the above-referenced application, even if such language does not appear in the specification.

In *Parks*, the Board of Patent Appeals & Interferences indicated: "Clearly, the observation of a lack of literal support does not, in and of itself, establish a *prima facie* case for lack of adequate descriptive support under the first paragraph of 35 U.S.C. 112." (Citations omitted).

Notably, the negative limitation in *Parks,* "in the absence of a catalyst," was deemed to have basis in the original disclosure despite the fact that the disclosure never specifically excluded use of a catalyst. 30 USPQ2d at 1236-37. The Board reasoned, "[t]hroughout the discussion[,] which would seem to cry out for a catalyst if one were used, no mention is made of a catalyst . . ." Consequently, the Board reversed the examiner's 35 U.S.C. § 112, first paragraph, rejections of claims which included the negative limitation at issue.

In the above-referenced application, support for etchants "consisting essentially of" $C_2H_xF_y$ and at least one fluorocarbon is provided at several locations, including page 8, lines 18-27; page 8, line 28, to page 9, line 6; page 9, lines 12-18; page 10, lines 1-6; and page 10, lines 7-12.

Nowhere does the specification of the above-referenced application mention an etchant which includes a component other than those recited in claims 1 and 20 that would "'not materially alter the novel and basic characteristics' of the claimed invention." In fact, in describing examples of inventive etchants, the specification does not mention anything other than a $C_2H_xF_y$ component and one or more fluorocarbons. The only mention of anything other than these two types of components is made, at page 10, lines 14-16, where use of a carrier gas with

the etchant is mentioned. As is well known in the art, a carrier gas is not part of the etchant, but merely facilitates delivery thereof to the substrate to be etched. In this regard, the specification of the above-referenced application, at page 12, lines 10-12, that the etchant may be introduced into an etch chamber with or without a carrier gas.

It is, therefore, respectfully submitted that the specification of the above-referenced application provides an adequate written description of the subject matter recited in claims 1 and 20. Accordingly, withdrawal of the 35 U.S.C. § 112, first paragraph, rejections of these claims, as well as of the claims depending therefrom, is respectfully requested.

Claim 18 has been rejected because the specification of the above-referenced application purportedly fails to provide an adequate written description for the recitation of an etchant that includes a first component and a primary etchant "etches doped silicon dioxide at a same rate as" doped silicon dioxide is etched by another "etchant that includes [the] primary etchant but not the first component." Support for this recitation is provided, for example, at page 9, lines 19-22, of the specification of the above-referenced application, which describes an etchant that "permit[s] [a] doped silicon dioxide etch to proceed at a substantially normal rate." Therefore, withdrawal of the 35 U.S.C. § 112, first paragraph, rejection of claim 18 is respectfully requested.

Claims 42 and 46 have been rejected for reciting "including at least one carrier gas," which is assertedly new matter. As noted previously herein, the specification describes use of carrier gases with the novel etchants. *See, e.g.,* page 10, lines 14-16; page 12, lines 10-12. As support for the subject matter recited in claims 42 and 46 has been provided in the specification of the above-referenced application, withdrawal of the 35 U.S.C. § 112, first paragraph, rejections of these claims is respectfully requested.

Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 1, 2, 4, 5, and 7-46 stand rejected under 35 U.S.C. § 112, second paragraph, for purportedly being indefinite.

More specifically, these claims have been rejected because independent claims 1 and 20 recite consisting essentially of, close-ended term, but are modified by open-ended claims.

It is respectfully submitted that the recitation of "comprising" in the dependent claims cannot negate the effect of the recitation of "consisting essentially of" in the independent claims. The independent claims recite dry etchants that consist essentially of one or more particular elements. Of the elements recited, *at least one* fluorocarbon is included. By reciting what the *at least one* fluorocarbon "comprises," the dependent claims merely introduce additional limitations; the use of "comprising" in the dependent claims does not make it possible for the *at least one* fluorocarbon of the independent claims to include anything other than (besides nonessential components) one or more fluorocarbons.

Therefore, it is respectfully submitted that claims 1, 2, 4, 5, and 7-46 comply with the requirements of the second paragraph of 35 U.S.C. § 112. Accordingly, it is respectfully submitted that each of these claims is in condition for allowance and requested that the 35 U.S.C. § 112, second paragraph, rejections of these claims be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

Claims 1, 2, 4, 5, and 7-46 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in U.S. Patent 5,814,563 to Ding et al. (hereinafter "Ding"), in view of teachings from U.S. Patent 5,626,716 to Bosch et al. (hereinafter "Bosch").

M.P.E.P. § 706.02(j) sets forth the standard for a rejection under 35 U.S.C. § 103(a):

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

With respect to rejections under 35 U.S.C. § 103(a) that are based upon references which qualify as prior art under 35 U.S.C. § 102(e), 35 U.S.C. § 103(c) provides:

> Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Bosch teaches a dry etch process in which a chemical combination that includes CHF_3 (Freon-23) and neon (Ne) is used to remove doped silicon oxide with selectivity over undoped silicon oxide, silicon nitride, silicide, and silicon. *See, e.g.,* col. 2, lines 34-44. Any of these materials may, therefore, be used as an etch stop when a doped silicon oxide is being dry etched with the disclosed combination of CHF_3 and Ne. *See, e.g.,* col. 4, lines 43-48. Bosch does not disclose, teach, or suggest any dry etchant chemical combination that includes $C_2H_xF_y$, where x is an integer from three to five, inclusive, y is an integer from one to three, inclusive, and $x + y = 6$. Nor does Bosch disclose, teach, or suggest that any such dry etchant chemical combination may be used to dry etch doped silicon oxide with selectivity over undoped silicon oxide or even that doped silicon oxide may be dry etched with such a chemical combination.

Bosch also repeatedly emphasizes the importance of including Ne in the dry etchant. *See, e.g.,* col. 2, lines 45-48; col. 5, lines 38-41; col. 6, lines 13-28. More specifically, Bosch teaches that Ne imparts the dry etchant mixtures disclosed therein with selectivity. In this regard, Bosch teaches that Ne is an essential ingredient of the dry etchants disclosed therein. *See id., see also* col. 5, lines 34 & 35.

Ding teaches, among other things, a dry etch process in which a chemical combination that includes a fluorocarbon gas, an ammonia-generating (NH_3-generating) gas, and a carbon-oxygen gas is used to dry etch dielectric materials such as doped and undoped silicon dioxide. *See, e.g.,* col. 2, lines 32-43. Ding also teaches that, by use of the chemical combination disclosed therein, dielectric materials, such as doped and undoped silicon oxides, may be removed with selectivity over underlying substrate materials, such as silicon or gallium arsenide. *See, e.g.,* col. 3, lines 49-54. Ding further provides that the dry etchant chemical combination

etches dielectric materials with selectivity over both photoresist materials and polysilicon. Col. 7, lines 44-49. Among the various fluorocarbons that are specifically disclosed in Ding as being useful in the chemical combination are CHF_3 and $C_2H_4F_2$. *See, e.g.,* col. 2, line 62, to col. 3, line 2.

Ding teaches that the ammonia-generating gas is an essential part of the dry etchant mixture disclosed thereon. *See, e.g.,* col. 6, lines 14-50.

Independent claim 1 recites a dry etchant which *consists essentially of* a first component and a second component. The first component of the dry etchant recited in independent claim 1 has the general formula $C_2H_xF_y$, where x is an integer from three to five, inclusive, y is an integer from one to three, inclusive, and $x + y = 6$. The second component of the dry etchant of amended independent claim 1 consists of at least one fluorocarbon. The dry etchant is formulated to etch doped silicon dioxide with selectivity over at least undoped silicon dioxide.

Independent claim 20 recites a dry etchant which consists essentially of at least one fluorocarbon. The at least one fluorocarbon of amended independent claim 20 includes a component which comprises $C_2H_xF_y$, where x is an integer from three to five, inclusive, y is an integer from one to three, inclusive, and $x + y = 6$. In addition, amended independent claim 20 recites that the dry etchant thereof is formulated to etch doped silicon dioxide at a faster rate than at least undoped silicon dioxide.

It is respectfully submitted that Ding and Bosch do not support a *prima facie* case of obviousness against any of claims 1-38 since Bosch and Ding both teach away from the subject matter recited in claims 1-38.

In particular, Bosch teaches a dry etchant combination which, in addition to a fluorocarbon, must also include Ne. *See, e.g.,* col. 2, lines 45-48; col. 5, lines 34 & 35; col. 5, lines 38-41; col. 6, lines 13-28. Ding teaches a dry etchant combination which requires one or more fluorohydrocarbon gases, one or more NH_3-generating gases, and a carbon-oxygen gas. Col. 2, lines 37-43; col. 2, lines 52-61.

In contrast, independent claim 1 recites a dry etchant which *consists essentially of* a first component comprising $C_2H_xF_y$, where x is an integer from three to five, inclusive, y is an integer from one to three, inclusive, and $x + y = 6$, and a second component consisting of at least one fluorocarbon. While this language does not exclude the presence of components, such as a carrier gas, which are not essential to the characteristics of the recited dry etchant, it does exclude other components, such as an NH_3-generating gas or a carbon-oxygen gas, that would materially alter the characteristics of the recited dry etchant. *See* M.P.E.P. § 2111.03. In fact, Ding, at col. 2, lines 46-51, notes that the NH3-generating gas is at least partially responsible for accelerated dielectric etch rates when a photoresist is also present.

Likewise, independent claim 20 is drawn to a dry etchant which *consists essentially of* at least one fluorocarbon.

As Bosch and Ding teach dry etchants which include fluorocarbons, as well as additional, nonfluorocarbon ingredients which are essential to the desired functions of such dry etchants, these references both teach away from the subject matter recited in amended independent claims 1 and 20, it is respectfully submitted that the subject matter recited in these claims is allowable over the combination of Ding and Bosch.

Due to the presence of additional ingredients in the dry etchants taught in Bosch and Ding, one of ordinary skill in the art could not reasonably expect the asserted combination of teachings from Bosch and Ding to successfully result in the claimed subject matter.

Moreover, as Bosch and Ding both teach dry etchant mixtures which include something more than fluorocarbons, it is respectfully submitted that neither Bosch nor Ding, taken separately or together, teaches or suggests a dry etchant that *consists essentially of* either the elements recited in independent claim 1 or those recited in independent claim 20.

Claims 2, 4, 5, 7-19, and 39-42 are each allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Claims 21-38 and 43-46 are each allowable, among other reasons, for depending either directly or indirectly from claim 20, which is allowable.

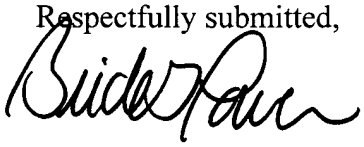
In view of the foregoing, it is respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 1, 2, 4, 5, or 7-46.

For these reasons, withdrawal of the 35 U.S.C. § 103(a) rejections of claims 1, 2, 4, 5, and 7-46 is respectfully requested.

CONCLUSION

It is respectfully submitted that each of claims 1, 2, 4, 5, and 7-46 is allowable. An early indication of the allowability of each of these claims and an indication that the above-referenced application has been passed for issuance are respectfully solicited. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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Supplemental Information Disclosure Statement (2 pages) along with Form PTO-1449 (1 page), with cited references (3 documents).

Invention ETCHANT WITH SELECTIVITY FOR DOPED SILICON DIOXIDE OVER UNDOPED SILICON DIOXIDE AND SILICON NITRIDE, PROCESSES WHICH EMPLOY THE ETCHANT, AND STRUCTURES FORMED THEREBY
Applicants Ko et al.
Filing Date November 13, 2000
Serial No. 09/711,324
Date Sent January 3, 2002 via Express Mail Label No. EL740545402US
Client/Matter Docket No. 2269/3526.4US
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Ko et al.

Serial No.: 09/711,324

Filed: November 13, 2000

For: ETCHANT WITH SELECTIVITY FOR DOPED SILICON DIOXIDE OVER UNDOPED SILICON DIOXIDE AND SILICON NITRIDE, PROCESSES WHICH EMPLOY THE ETCHANT, AND STRUCTURES FORMED THEREBY

Examiner: K. Chen

Group Art Unit: 1765

Attorney Docket No.: 3526.4US (97-1136.4)

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 be considered by the Examiner and made of record. The listed documents are from co-pending application Serial No. 09/610,049, filed July 5, 2000. Copies of the listed documents are enclosed pursuant to 37 C.F.R. § 1.98(a).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other

possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

DOCUMENTS

U.S. Patent Documents

U.S. Patent No.	Issue Date	Inventor
5,828,096	10/1998	Ohno et al.
5,831,899	11/1998	Wang et al.

Other Documents

Wolf, Stanley, "Silicon Processing for the VLSI Era," cover pages and pages 194-195, Volume 2: Process Integration.

Applicants offer to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed after the mailing date of the final Office Action under 37 C.F.R. § 1.113, but before payment of the issue fee. I hereby certify that no item of information contained in the Supplemental Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of the statement, therefore no fee pursuant to 37 C.F.R. § 1.17(i) is required.

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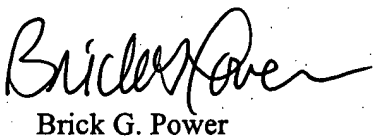

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

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Applicant K t al.	
Filing Date November 13, 2000	Group Art Unit 1765

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5,828,096	10/1998	Ohno et al.			
	5,831,899	11/1998	Wang et al.			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

		Wolf, Stanley, "Silicon Processing for the VLSI Era," cover pages and pages 194-195, Volume 2: Process Integration.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

SILICON PROCESSING

FOR

THE VLSI ERA

VOLUME 2:

PROCESS INTEGRATION

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Table 4.4 Desired Properties of Interlevel Dielectrics for VLSI[11]

1. Low *dielectric constant* for frequencies up to ~20 MHz, in order to keep capacitance between metal lines low.
2. High breakdown field strength (>5 MV/cm).
3. Low leakage, even under electric fields close to the breakdown field strength. Bulk resistivity should exceed 10^{15} Ω-cm.
4. Low surface conductance. Surface resistivity should be $>10^{15}$.
5. No moisture absorption or permeability to moisture should occur.
6. The films should exhibit low stress, and the preferred stress is compressive (~5×10^8 dynes/cm^2), since dielectric films under tensile stress exhibit more of a tendency to crack.
7. Good adhesion to aluminum, and of aluminum to the dielectric. (Good adhesion is also needed to the other conductors used in VLSI, such as doped polysilicon and silicides). In cases of poor adhesion (such as with gold or CVD W), a glue layer (such as Ti or Ti:W) may need to be applied between the conductor and the dielectric.
8. Good adhesion to *dielectric layers* above or below. Such dielectric layers could be thermal oxides, doped-CVD oxides, nitrides, oxynitrides, polyimides, or spin-on glasses.
9. Stable up to temperatures of 500°C.
10. Easily etched (by wet or dry processing).
11. Permeable to hydrogen. This is important for IC processing, in which an anneal in a hydrogen containing ambient must be used to reduce the concentration of interface states between Si and the gate oxides of MOS devices (see Vol. 1, chap. 8).
12. No incorporated electrical charge or dipoles. Some polyimides in particular contain polar molecules that can orient themselves in an electric field and give rise to an electric field even when the externally applied field is removed.
13. Contains no metallic impurities.
14. Step coverage that does not produce reentrant angles.
15. Good thickness uniformity across the wafer, and from wafer to wafer.
16. In the case of doped oxides, good dopant uniformity across the wafer, and from wafer to wafer.
17. Low defect density (pinholes and particles).
18. Contains no residual constituents that outgas during later processing to the degree that they degrade the properties of other layers of the interconnect system (e.g., outgassing from some polyimide films, SOG films, or low-temperature TEOS films).

Silane-based phosphorus-doped SiO_2 films deposited at low temperatures (350-450°C) have also been used as PMD layers. The addition of phosphorus to the films allows reflow to be performed at ~1000°C in steam. However, the need for lower flow and reflow temperatures has made silane-based BPSG and boron/phosphorus-doped TEOS films more attractive.[13] Reflow temperatures of less than 850°C can be achieved with BPSG.

etching problem to be circumvented by selectively depositing the Cu; device contamination can be controlled by utilizing silicon nitride under the Cu lines; and corrosion can be stopped by selectively covering the Cu lines with a layer of nickel.

4.3.2 Dielectric Materials for Multilevel Interconnects

4.3.2.1 Requirements of Dielectric Layers in Multilevel Interconnects. Dielectric layers must be used to electrically isolate one level of conductor from another in multilevel-interconnect systems. The list of properties that must be possessed by such dielectric layers is given in Table 4-4. As is the case for conductor materials used in such applications, the list of requirements is long and stringent. When we describe the materials that have been developed for this role, Table 4-4 will serve as our point of reference.

It should also be mentioned that there can be a significant difference between the dielectric film referred to in Fig. 4-7 as PMD (used between polysilicon, or other local-interconnect level material, and Metal 1) and the dielectric films that are employed between the metal layers (*intermetal dielectrics* – e.g., DM1 in Fig. 4-7). PMD films can be deposited (and densified if necessary) at a higher temperature than is possible for the intermetal dielectric layers. Furthermore, PMD films can be *flowed* and *reflowed* at temperatures in excess of 800°C. On the other hand, when Al is present on the wafer surface, the maximum temperature of the intermetal dielectric layers is limited to ~450°C. We will therefore discuss these two dielectric types separately, even though some dielectric films can be used for both applications.

4.3.2.2 Poly-Metal Interlevel Dielectric (PMD) Materials. Doped CVD SiO_2 films have found the widest application as PMD layers in MOS ICs. Silicon nitride films have generally not been used as stand-alone PMD layers because they possess a much higher dielectric constant than SiO_2 films and because they cannot be flowed or reflowed. High-temperature CVD-oxide films (deposited at 900°C by the reaction of dichlorosilane and nitrous oxide) were among the first materials used for this purpose. Such films provide excellent step coverage, as well as dielectric properties almost identical to those of thermally grown SiO_2 films (see Vol. 1, chap. 6). Unfortunately, these films cannot be doped because of the high temperature at which they are deposited; as a result, they cannot be flowed or reflowed at temperatures lower than 1100°C.

Undoped TEOS films (deposited by the decomposition of *tetraethyl orthosilicate* [TEOS] at 600-650°C) were also used as PMD layers in some early IC processes because of their excellent step coverage. In order to allow such TEOS films to be reflowed, phosphorus- and boron-doped TEOS deposition processes were subsequently developed. Recent efforts with doped-TEOS processes have been aimed at replacing the relatively toxic phosphine and diborane dopant gases with less toxic liquid sources.[12] In addition, PECVD TEOS processes have recently been developed in which TEOS films can be deposited at lower temperatures (e.g., 375°C; see section 4.3.2.4).

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Invention:	ETCHANT WITH SELECTIVITY FOR DOPED SILICON DIOXIDE OVER UNDOPED SILICON DIOXIDE AND SILICON NITRIDE, PROCESSES WHICH EMPLOY THE ETCHANT, AND STRUCTURES FORMED THEREBY
Applicant(s):	Ko et al.
Filing Date:	November 13, 2000
Serial No.:	09/711,324
Date Sent:	June 26, 2003 via first class mail
Docket No.:	2269-3526.4US
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In re Application of:

Ko et al.

Serial No.: 09/711,324

Filed: November 13, 2000

For: ETCHANT WITH SELECTIVITY FOR DOPED SILICON DIOXIDE OVER UNDOPED SILICON DIOXIDE AND SILICON NITRIDE, PROCESSES WHICH EMPLOY THE ETCHANT, AND STRUCTURES FORMED THEREBY

Confirmation No.: 7008

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Group Art Unit: 1765

Attorney Docket No.: 2269-3526.4US
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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

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Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 be considered by the Examiner and made of record. Copies of the listed documents are enclosed pursuant to 37 C.F.R. § 1.98(a).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

U.S. Patent No.	Publication Date	Patentee
4,529,476	07/1985	Kawamoto et al.
6,018,184	01/2000	Becker
6,066,555	05/2000	Nulty et al.
6,110,831	08/2000	Cargo et al.
6,117,791	09/2000	Ko et al.
6,277,720 B1	08/2001	Doshi et al.
6,303,496 B1	10/2001	Yu
6,483,172 B1	11/2002	Cote et al.

Foreign Patent Documents

Document No.	Publication Date	Patentee
61251138	08/1986	JP
0721205 A2	07/1996	EPO
WO 98/49719	11/1998	PCT

Other Documents

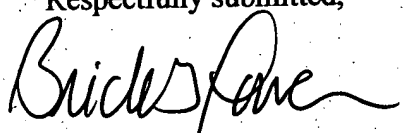
Wolf, S., et al., Silicon Processing for the VLSI Era, Vol. 1, Process Technology, Lattice Press, 1986, pp. 520-523.
Williams, K., BSAC Etch Rates for Micromachining and IC Processing, U.C. Berkeley Microfabrication Lab., Berkeley Sensor & Actuator Center, http://www-bsac.eecs.berkeley, edu/db/etchrates.html.
Williams, K., VLSI Etchants, Chapter 1.5, Rev. 11/97, http://microlab.berkeley,edu/labmanual/chap1/1.5.html.

Applicants offer to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed after the mailing date of the first Office Action on the merits.

The fee pursuant to 37 C.F.R. § 1.17(p) is enclosed.

Respectfully submitted,



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Form PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION *(Use several sheets if necessary)*	Docket Number (Optional) **3526.4US (97-1136.05/US)**	Application Number **09/711,324**
	Applicant **Ko et al.**	
	Filing Date **November13, 2000**	Group Art Unit **1765**

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4,529,476	07/1985	Kawamoto et al.			
	6,018,184	01/2000	Becker			
	6,066,555	05/2000	Nulty et al.			
	6,110,831	08/2000	Cargo et al.			
	6,117,791	09/2000	Ko et al.			
	6,277,720 B1	08/2001	Doshi et al.			
	6,303,496 B1	10/2001	Yu			
	6,483,172 B1	11/2002	Cote et al.			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO
	61251138	08/1986	JP			X	
	0721205 A2	07/1996	EPO				
	WO 98/49719	11/1998	PCT				

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Wolf, S., et al., Silicon Processing for the VLSI Era, Vol. 1, Process Technology, Lattice Press, 1986, pp. 520-523.
	Williams, K., BSAC Etch Rates for Micromachining and IC Processing, U.C. Berkeley Microfabrication Lab., Berkeley Sensor & Actuator Center, http://www-bsac.eecs.berkeley.edu/db/etchrates.html.
	Williams, K., VLSI Etchants, Chapter 1.5, Rev. 11/97, http://microlab.berkeley.edu/labmanual/chap1/1.5.html.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Includ copy of this form with next communication to the applicant.

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(11) Publication number: **61251138 A**

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PATENT ABSTRACTS OF JAPAN

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(74) Representative:

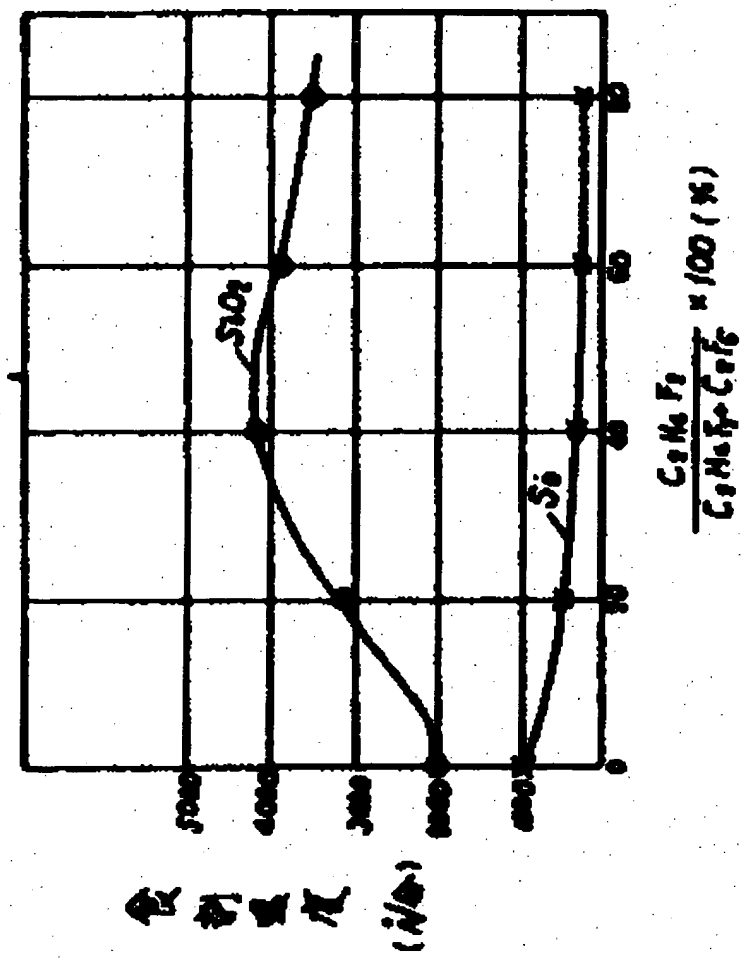
(54) DRY ETCHING

(57) Abstract:

PURPOSE: To reduce a polymer of CF2 and etch silicon dioxide without damaging a silicon foundation layer by exposing the silicon dioxide to the plasma of a mixed gas composed of a CF system gas and C2H4F2.

CONSTITUTION: A silicon dioxide film of 4,000Å is formed on a silicon substrate and this film is etched by an etching apparatus in which the pressure can be maintained constant at 500mTorr using a mixed gas composed of C2F6 and C2H4F2. According to the results of the experiments by varying the ratio of mixing of the mixed gas while a high frequency power of 500W is being applied between a parallel plane electrodes, when the ratio of C2H4F2 is 0%, the etching rate is 1,000Å/min. for Si and 2,000Å/min. for SiO2, when the ratio of C2H4F2 is 10% or higher, the etching rate is 500Å/min. or

less for Si and 3,000Å/min. or more for SiO2 and, when the ratio of C2H4F2 is 40%, the etching rate is 210Å/min. for Si and 4,200Å/min. for SiO2.



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(54) Method of etching an oxide layer with simultaneous deposition of a polymer layer

(57) A method of etching an oxide layer is disclosed. First, a resist layer is formed on an oxide layer on a substrate. Next, a photosensitive layer is formed on the oxide layer and patterned to expose regions of the oxide layer to be removed. The exposed regions may overlie a nitride layer, and may overlie a structure such as a polysilicon gate. The etch is performed such that polymer deposits on the photosensitive layer, thus eliminating interactions between the photosensitive layer and the plasma. In this way, a simple etch process allows for good control of the etch, resulting in reduced aspect ratio dependent etch effects, high oxide:nitride selectivity, and good wall angle profile control.

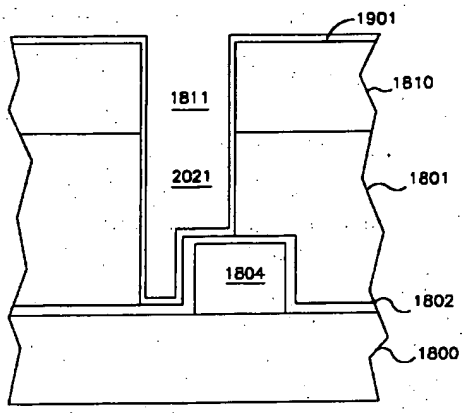

FIG. 20

EP 0 721 205 A2

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Descripti n

This application is a continuation-in-part of United States patent application Serial No. 08/234,478, filed April 28, 1994, which application is assigned to the assignee of the present application.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of semiconductor device fabrication and more particularly to improved methods for etching openings in oxide layers.

2. Background Information

In the fabrication of semiconductor devices, numerous conductive device regions and layers are formed in or on a semiconductor substrate. The conductive regions and layers of the device are isolated from one another by a dielectric, for example, silicon dioxide. The silicon dioxide may be grown, or may be deposited by physical deposition (e.g., sputtering) or by a variety of chemical deposition methods and chemistries. Additionally, the silicon dioxide may be undoped or may be doped, for example, with boron, phosphorus, or both, to form for example, borophosphosilicate glass (BPSG), and phosphosilicate glass (PSG). The method of forming the silicon dioxide layer and the doping of the silicon dioxide will depend upon various device and processing considerations. Herein, all such silicon dioxide layers are referred to generally as "oxide" layers.

At several stages during fabrication, it is necessary to make openings in the dielectric to allow for contact to underlying regions or layers. Generally, an opening through a dielectric exposing a diffusion region or an opening through a dielectric layer between polysilicon and the first metal layer is called a "contact opening", while an opening in other oxide layers such as an opening through an intermetal dielectric layer (ILD) is referred to as a "via". As used herein, an "opening" will be understood to refer to any type of opening through any type of oxide layer, regardless of the stage of processing, layer exposed, or function of the opening.

To form the openings, a patterning layer of photoresist is formed over the oxide layer having openings corresponding to the regions of the oxide where the oxide layer openings are to be formed. In most modern processes a dry etch is performed wherein the water is exposed to a plasma, formed in a flow of one or more gases. Typically, one or more halocarbons and/or one or more other halogenated compounds are used as the etchant gas. For example, CF_4, CHF_3(Freon 23), SF_6, NF_3, and other gases may be used as the etchant gas. Additionally, gases such as O_2, Ar, N_2, and others may be added to the gas flow. The particular gas mixture used will depend on, for example, the characteristics of the oxide being etched, the stage of processing, the etch tool being used, and the desired etch characteristics such as, etch rate, wall slope, anisotropy, etc.

Various etch parameters such as the gas mixture, temperature, RF power, pressure, and gas flow rate, among others, may be varied to achieve the desired etch characteristics described above. However, there are invariably tradeoffs between the various desired characteristics. For example, most high performance etches exhibit aspect ratio dependent etch effects (ARDE effects). That is, the rate of oxide removal is dependent upon the aspect ratio of the opening, which can be defined as the ratio of the depth of the opening to the diameter. In general, the oxide etch rate, in terms of linear depth etched per unit time, is much greater for low aspect ratio openings than for high aspect ratio openings. Referring to Figure 1, substrate 100 represents a semiconductor substrate and any device layers or structures underlying the oxide layer 101 through which the etch is to be performed. For example, there may be a silicon nitride layer (Si_3N_4) underlying oxide layer 101. Herein, the term silicon nitride layer or nitride layer is used generally to refer to a layer of Si_xN_y, wherein the ratio x:y may or may not be stoichiometric, as well as to various silicon oxynitride films ($Si_xO_yN_z$).

As shown, patterning layer 110, which may be a photoresist layer, comprises openings 111 and 112. As can be seen, the diameter of opening 112 is much smaller than that of opening 111. Since the thickness of oxide layer 101 is the same under both openings, the oxide opening under photoresist opening 112 will have a much greater aspect ratio due to its small diameter. As a result of this, as shown in Figure 1, the prior art etch process causes opening 121 through the oxide layer 101 to be fully etched prior to opening 122. In the prior art, this aspect ratio dependency may be overcome by adjusting the feed gas chemistry, adjusting the operating pressure, increasing the pumping speed to allow for high flow/low pressure operation, and the addition of diluent gases. However, in addition to the cost and time involved in the redesign of the process, these methods of minimizing the aspect ratio dependency typically result in a tradeoff between ARDE effects and other characteristics such as etch rate, selectivity, and profile control, for example. Recently, use of high density plasma (HDP) systems has been proposed to compensate for the ARDE effect. However, these HDP systems are not yet proven in a production mode, and they entail significant capital costs. It should be noted that more advanced technologies demand high etch performance in high aspect ratio features, and demand high etch performance in layers having features with a wide range of aspect ratios. Thus, the ARDE effect constitutes a significant hurdle in advanced applications.

Many of the etch characteristics are generally believed to be affected by polymer residues which deposit during the etch. For this reason, the fluorine to carbon ration (F/C) in the plasma is considered an important determinant in the etch. In general, a plasma with a high F/C ratio will have a faster etch rate than a plasma

with a low F/C ratio. At very low ratios, (i.e., high carbon content) polymer deposition occurs and etching ceas s. The etch rate as a function of the F/C ratio is typically different for different materials. This difference is used to create a selective etch, by attempting to use a gas mixture which puts the F/C ratio in the plasma at a value that leads to etching at a reasonable rate for one material, and that leads to no etching or polymer deposition for another. For a more thorough discussion of oxide etching, see S. Wolf and R.N. Tauber, Silicon Processing for the VLSI Era, Volume 1, pp 539-585 (1986).

By adjusting the feed gases, the taper of the sidewall of the oxide opening can be varied. If a low wall angle is desired, the chemistry is adjusted to try to cause some polymer buildup on the sidewall. Conversely, if a steep wall angle is desired, the chemistry is adjusted to try to prevent buildup on the sidewall. An important problem with changing the etch chemistry is that there is a tradeoff between wall angle and selectivity. That is, etches which provide a near 90° wall angle are typically not highly selective between oxide and an underlying silicon or silicon nitride layer, for example, while highly selective etches typically have a low wall angle.

Figure 2 shows an oxide layer 201 formed on substrate 200, having patterning layer 210 with opening 211 therein. Opening 221 in the oxide layer 201 is shown during formation. In the etch illustrated in Figure 2, high selectivity may be desired to protect an underlying region of, for example, silicon nitride on the upper surface of substrate 200. It also may be desired to obtain a relativity straight profile. However, if selectivity is to be maintained, the resulting opening 221 will have a taper as shown by angle 206. Often, in a prior art etch with acceptable selectivity, the angle 206 is less than 85°. This tradeoff is particularly severe in etches through thick oxide layers. For example, if the process is engineered to allow for a steep wall profile through a thick BPSG layer, the selectivity will be very poor. While adjustments can be made to improve the wall angle, such as by changing etch chemistry, and other parameters, all processes will suffer from the selectivity tradeoff to some degree. Additionally, such changes will affect other performance goals. For example, as mentioned above, adjustment to the process parameters will have some effect on the ARDE effect. Furthermore, even if adjustments to the etch parameters are found which enhance selectivity without a severe impact on wall angle, such adjustments will involve other tradeoffs. For example, there is typically a tradeoff between selectivity and etch rate, so that increased selectivity may only be had at the expense of throughput. As can be seen, though some adjustments can be made, it is extremely difficult to design an oxide etch which meets all necessary goals. Additionally, it will be appreciated that while the general effects of certain process conditions are known, and the existence of certain tradeoffs can be predicted, it is far from a straightforward matter to precisely tailor an etch or precisely predict the effects changes in the parameters will have. Furthermore, it is often difficult t prevent other undesired consequences of polymer buildup.

Figure 3 illustrates the effect of polymer buildup during a typical prior art etch process. Polymer buildup along the regions 307 along the sidewalls of opening 321 cause the wall profile to be different than a straight etch profile, shown dashed. Additionally, polymer buildup in the region 308 at the center of the bottom of the opening prevents etching of a portion of the nitride layer 302. However, etching does occur around the outer edges. Thus, the result of the prior art process is poorly controlled wall profile, and non-uniformity of the nitride layer 302 in the bottom of the opening 321. Again, changing the gas chemistry and other etch parameters may be used to improve the etch, but some tradeoffs are inevitable. Additionally, for example, attempts to improve the oxide:nitride selectivity often lead to non-stable plasma conditions, and involve high polymer chemistries, which in turn leads to dirty reactors requiring extensive maintenance, and particle generation which reduces yields.

The above described difficulties in oxide etching make it extremely difficult to form openings over corners of structures. Referring to Figure 4, opening 411 in patterning layer 410 is aligned to partially overlie structure 404, which may be, for example, a gate, an interconnect line, or other structure. As shown, structure 404 is covered by silicon nitride etch stop layer 403. Typically, the opening 421 is designed to partially overlie structure 404 to a certain extent. Note that as the etch proceeds, opening 421 will extend to the corner of the structure 404 prior to the completion of the etch to the bottom of the opening at 432. As shown, due to the difficulty in achieving a highly selective etch, the nitride layer 403 is removed from structure 404 on the top 430 and side 431, which are exposed to the etch for a significant time before the etch reaches the bottom 432. This problem is particularly severe if the opening 411 is misaligned such that the opening in the oxide layer is formed as shown by dashed lines 421a. The opening 421a exposes a smaller area of nitride layer 403 than the opening 421. This leads to a reduction in the micro-loading effect, which in turn causes the now reduced area of nitride layer 403 to be etched at a much faster rate.

What is needed is a method or methods of etching oxide with reduced ARDE effect, which exhibit a high oxide to nitride selectivity, and which provide control of wall profile. Further, it is preferable that any such methods do not suffer from severe tradeoffs between and among these and other performance goals such as etch rate, so that highly selective etches with reduced sidewall taper and/or reduced ARDE effects, may be achieved. The method or methods should enable the formation of openings which lie on or over other structures, such as in a self-aligned contact etch. Finally, the method or methods should allow for increased opening depth, especially in process steps requiring the formation of deep openings of different depths, without an unacceptable sacrifice in performance. The method or methods should provide the above described etch characteristics

without requiring extensiv redesign of the process or process tools, unacceptable performance or process maintenance trad offs, costly and unproven equipment, or high particle generation.

SUMMARY OF THE INVENTION

A method of etching openings such as contact openings or via openings in an oxide layer is disclosed. The method of the present invention may be used for a wide variety of etches, including etches with openings having different aspect ratios, over flat structures, over steep topography, and in etches having all of these. In the present invention, the ARDE effect is reduced or eliminated, improved oxide:nitride selectivity is achieved, and tradeoffs between selectivity and other performance goals are greatly reduced or eliminated. In one embodiment, a hard mask layer of, for example, polysilicon is used as a mask for the oxide etch. A patterned photoresist layer, exposing regions of the hard mask corresponding to the openings to be formed in the oxide layer is formed on the hard mask. An etch of the hard mask in the exposed regions is then performed. It has been found that the interaction of the photoresist mask, and more particularly it is believed the carbon from the photoresist mask, with the plasma etch chemistry has a dominant effect on the aspect ratio dependency of the etch. Therefore, in one embodiment, the photoresist mask is removed prior to the completion of the oxide etch. The elimination of the photoresist/etch chemistry interaction has been found to greatly reduce or eliminate aspect ratio dependent etch effects. Additionally, the hard mask is found to interact with the etch chemistry to improve the oxide:nitride selectivity. In another embodiment of the present invention, the oxide etch is carried out at an elevated temperature, allowing for increased selectivity without a tradeoff with wall angle. In a further embodiment, Freon 134a is used as an additive to the etchant gas allowing for improved oxide:nitride selectivity. In a further embodiment, the hard mask, Freon 134a, and elevated temperature are used to perform etches providing a selective oxide:nitride etch over both flat surfaces and corner topography. In additional embodiments, the etches may be carried out in two steps. In the case of a thick oxide layer, this allows for a high etch rate, and selectivity, while leaving a uniform nitride underlayer. In one two step etch process, a clean step is performed to remove any built up polymers before proceeding with the second etch step.

In a further embodiment of the present invention, an etch is performed using a photoresist mask. This etch is carried out such that a polymer deposits on the resist surface, and additionally, the side walls of the openings as they are being formed. In this way, the photoresist mask does not interact with the plasma, thus providing for greatly reduced or eliminated aspect ratio dependent etch effects. Further, the etch chemistry results in improved oxide:nitride selectivity. This etch may be used over both flat or cornered topographies without the need for a separate hard mask deposition and etch step.

Additional features and benefits of the present invention will become apparent from the detailed description, figures, and claims set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings in which like references indicate similar elements and in which:

Figure 1 illustrates aspect ratio dependent etching of a prior art oxide etch process.

Figure 2 illustrates wall profile in a prior art oxide etch process.

Figure 3 illustrates poor oxide:nitride selectivity in a prior art etch process.

Figure 4 illustrates a prior art etch process over a structure.

Figure 5 is a cross-sectional election view of a structure having a hard mask of one embodiment of the present invention.

Figure 6 illustrates the structure of Figure 5 after the etch of the hard mask.

Figure 7 illustrates the oxide etch performed on the structure of Figure 6 in an embodiment of the present invention, just prior to completion.

Figure 8 shows a block diagram of the steps used in the process shown in Figures 5 - 7.

Figure 9 illustrates the result of an oxide etch in accordance with an embodiment of the present invention.

Figure 10A illustrates the molecular structure of an etchant used in an embodiment of the present invention.

Figure 10B illustrates a proposed reaction of the molecule of Figure 10A.

Figure 11 shows the result of an oxide etch using a chemistry comprising the etchant shown in Figure 10.

Figure 12 illustrates a cross-sectional elevation view of a structure on which an oxide etch according to an embodiment of the present invention is to be performed.

Figure 13 illustrates th structure of Figure 12 after etching of the hard mask of an embodiment of the pres nt invention.

Figure 14 illustrates the structure of Figure 13 after an oxide etch according to an embodiment of the present invention.

Figure 15 illustrates a cross-sectional elevation view of a structure to be etched in an embodiment of the present invention.

Figure 16 shows the structure of Figure 15 after a first etch step and a clean step.

Figure 17 illustrates the structure of Figure 16 after a second etch step.

Figure 18 illustrates a cross-sectional elevation view of a structure to be etched in a further embodiment of the present invention.

Figure 19 illustrates the structure of Figure 18 during the etch.

Figure 20 illustrates the structure of Figures 18 and 19 at the completion of the etch.

DETAILED DESCRIPTION

A method of etching an oxide layer is disclosed. In the following description, numerous specific details are set forth such as specific materials, thicknesses, processing steps, process parameters, etc. in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that these specific details need not be employed to practice the present invention. In other instances, well known materials or methods have not been described in detail in order to avoid unnecessarily obscuring the present invention. Furthermore, in the following discussion, several embodiments of the present invention are illustrated with respect to specific structures, oxide layers, and oxide layer openings. It will be appreciated that each of the methods described herein can be utilized on a variety of structures and oxide layers, to form any type of opening, and each of the oxide etching methods described herein is not necessarily restricted to the structure and/or oxide layer in conjunction with which it is described. Further, any of the methods described herein may be performed as a part of a multistep etch comprising additional etch processes. Several exemplary multistep processes are described below.

Figures 5 - 7 illustrate a structure during fabrication according to a preferred embodiment of the present invention. Figure 8 shows a block diagram of the process shown in conjunction with Figures 5 - 7. First, as shown by block 801 of Figure 8, substrate 500 having oxide layer 501 thereon is formed, as illustrated in Figure 5. Substrate 500 may comprise a semiconductor substrate including device regions, layers, and structures, and may have varying topography underlying oxide layer 501. Oxide layer 501 may be any type of oxide, doped r undoped, and may be a grown oxide or a deposited oxide deposited by any method such as CVD, sputter deposition, etc. It will be appreciated that oxide layer 501 may be a multi-layer structure consisting of several different types of oxide layers. For example, in one embodiment, oxide layer 501 comprises a 10,000 Å BPSG layer, which itself may comprise several sublayers of different dopant concentrations, plus 3000 Å of undoped oxide on top of the BPSG layer. In one embodiment, the oxide layer 501 is disposed on a 900 Å CVD nitride layer comprising the uppermost surface of substrate 500. Then, in step 805 of Figure 8, a hard mask is formed on the oxide layer. As shown in Figure 5, hard mask layer 505 is deposited upon oxide layer 501. In a preferred embodiment, hard mask layer 505 comprises polysilicon deposited by, for example, CVD to a thickness in the range of approximately 500 - 5000 Å. It will be appreciated that hard mask layer 505 can be deposited by any well known method, and that other thicknesses may be used. Additionally, it will be appreciated that other types of layers or combination of layers may be used as the hard mask, such as silicon nitride, aluminum, titanium silicide, tungsten, or other refractory metal, etc. For reasons that will be seen, hard mask layer 505 is preferably a non-carbon or very low carbon contributing film.

In step 810, patterning layer 510 which may be, for example, photoresist, is deposited on hard mask layer 505 and patterned to form openings 511 and 512 using well known methods, as shown in Figure 5. It will be appreciated that many additional openings across the surface of the wafer may be formed simultaneously with those shown in the Figures. Next, in step 815 the hard mask is etched using an etchant appropriate for the material of which hard mask 505 is composed, and patterning layer 510 is removed in step 820. The resulting structure after steps 815 and 820 is shown in Figure 6 wherein openings 515 and 516 have been formed in hard mask layer 505. Note that the diameter of opening 515 is significantly greater than that of opening 516, so that opening 516 has a much higher aspect ratio. As described earlier, this typically leads to a much slower oxide etch rate in the region of opening 516. However, with use of the hard mask 505 this is avoided in the present invention. The structure of Figure 6 is next subjected to an oxide etch in step 805 to form openings in the oxide layer corresponding to hard mask openings 515 and 516. Referring to Figure 7, openings 521 and 522 in the oxide layer 501 during the etch, at a time just prior to completion of the etch, are shown. As can be seen, the openings 521 and 522 extend approximately the same distance through the oxide layer 501. Thus, by use of the hard mask, the ARDE effect is greatly reduced or eliminated. As mentioned above, substrate 500 may have varying topography, so that the openings through oxide layer 501 extend to varying depths. Therefore, in

such a case, even if all openings have the same diameter, there will be varying aspect ratios across the wafer due to the different depths. Additionally there may be both varying depths and varying diameters of openings. In all of these cas s, the hard mask of the present invention has been found to reduce or eliminate the aspect ratio dependency of the etch.

Although the use of hard mask 505 is advantageous in any etch process, one embodiment of the present invention is carried out in the LAM 384T Dry Etch System which is an RIE/Triode system. For 6" (150 mm) wafers, the etch is carried out in a flow comprising 2.5 standard cubic centimeters per minute (SCCM) Freon 134a and 10 SCCM CHF_3 (Freon 23). The etch is carried out at 600 watts (W) with a DC bias of approximately 1400 volts (V). The etch is performed at a pressure in the range of approximately 10 - 40 mTorr. The lower electrode water coolant temperature is set at 17° C, and the upper chamber temperature is set at 50° C. It will be appreciated that although the above described etch was performed in a single step after removal of the photoresist layer 510, the etch may be carried out in two steps, with a first portion of the oxide layer etched with resist layer 510 intact, followed by resist strip, and then a high performance final etch step with just the hard mask remaining to define the openings. For example, in one embodiment a high etch rate, non-selective etch step designed to etch the undoped oxide layer and some of the doped layer, such that there remains approximately 2000 Å of oxide in the thinnest area of the wafer, is first performed, followed by a second etch step similar to that described above. As will be described in a further embodiment of the present invention, a clean step may be performed between the etch steps.

The use of hard mask 505 as described above is beneficial in any existing oxide etch process. The invention is believed to provide for minimized ARDE effect by eliminating the photoresist contribution to the total carbon content of the plasma. As described earlier, polymer residue formed from carbon in the plasma has a strong effect on etch characteristics such as selectivity and wall profile. However, it is heretofore not been recognized that the photoresist layer has such a dominant effect on etch characteristics such as the ARDE effect. Because this dominant effect from the photoresist is removed, considerable process latitude is achieved, since the selection of the etch gas chemistry is no longer constrained by the requirement that it be adjusted to minimize the ARDE effect, and can instead be adjusted to achieve other performance goals such as etch rate, selectivity, profile control, etc. As described above, the benefits of the present invention are believed to be achieved by eliminating the interaction of the photoresist, and most likely the carbon from the photoresist, with the plasma chemistry. Therefore, in alternative embodiments of the present invention, a photosensitive layer which has been treated to become relatively inert to the plasma chemistry may be used as the sole masking layer. For example, a silylated photoresist layer, formed by, for example, a process known as the "DESIRE" process may be used. In this process, the exposed resist layer is treated with HMDS or a similar compound to impregnate portions of the layer with silicon. See, for exampl , Pavelch k et al., "Process Techniques For Improving Performance of Positive Tone Silylation" SPIE vol. 1925, pp 264 - 269, January 1993; and, C.A. Spence, S.A. MacDonald, and H. Schlosser, "Silylation Of Poly (t-BOC) Styrene Resists: Performance And Mechanisms," U.C. Berkeley and IBM Almaden Research Centre. See also, references cited in these papers. A photosensitive layer treated in this or a similar manner, which does not significantly react with the etch chemistry, and therefore does not overwhelm the carbon content of the plasma, may be used in place of the hard mask layer described herein. In this case, there is no need for both a patterning layer and a hard mask layer as described above. By inclusion of hard mask 505, or by making the photosensitive layer substantially inert to the plasma chemistry, an existing oxide etch process need not be reengineered, performed on new equipment, etc., and many of the tradeoffs associated therewith can be avoided or minimized. In the present invention, the etch can be tailored without the problem of carbon from the photoresist overwhelming the etch characteristics. As will be seen, embodiments of the present invention further include methods of minimizing the selectivity/wall angle tradeoff, improved oxide:nitride selectivity, improved selectivity in etches requiring openings to extend over corners, and methods of etching deep openings in the oxide layer. The methods of the present invention may be used to achieve the various performance goals as described generally herein, and may be used to improve process latitude.

As is well known, in the prior art methods of etching an oxide layer, considerable heat is generated by collisions of the ions and/or electrons in the plasma with the substrate. As is known, the amount of energy generated in this way will be dependent upon the various process parameters such as the gas used, power, etc. To prevent extreme temperature rises, the wafer temperature is controlled by a flow of a coolant such as water through the lower electrode, and/or by a flow of, for example, helium gas to the backside of the wafer. In typical processes, the cooling is carried out such that the wafer reaches a maximum temperature in the range of approximately 60° - 80° C. In any event, the upper temperature limit is constrained by the use of a photoresist patterning layer, since the wafer must be cooled sufficiently to prevent the resist temperature from exceeding the resist reticulation temperature, at which point the resist layer deforms, leading to loss of dimensional control, and potential openings in areas which are designed to remain unetched. Typical resists have a reticulation temperature of approximately 110° C. However, note that in the present invention, as shown in Figure 6, the resist layer may be removed prior to performing the oxide etch. Therefore, in a further embodiment of the present invention the temperature is adjusted (by appropriate adjustment of the backside coolant flow) above the resist

reticulation temperature if desired. For example, in one embodiment performed in the above described etch system, the backside helium pressure is reduced to approximately 2 Torr, which typically results in a helium flow of approximately 1 - 5 SCCM, as compared with approximately 8 Torr, which typically results in the helium flow of approximately 5 - 15 SCCM, for a similar process using a resist mask. By adjusting the helium pressure as described above, the wafer temperature can be expected to reach temperatures of approximately 100° - 200° C or higher. In a preferred embodiment, the wafer temperature is maintained at approximately 110 - 130° C. Note that this temperature range is above the resist reticulation temperature described above.

Figure 9 shows an example of opening 921 formed in oxide layer 901, which may be any type of oxide layer, using hard mask 905, which is generally similar to hard mask 505. The substrate 900 is generally similar to substrate 500, and may comprise many layers, structures, and may have topography underlying the openings to be formed. As before, a plurality of openings may be formed having different diameters and/or different aspect ratios. The etch is performed with the above described helium flow and pressure. In one embodiment the etch is performed in a flow comprising approximately 1.5 SCCM Freon 134a and approximately 47 SCCM CHF_3. The etch is carried out at a power of 600 W, a pressure of 30 mTorr, and a DC bias of approximately 1400 V. The lower electrode water coolant temperature is set at approximately 17° C and the upper chamber temperature is 50° C. The angle 906 using the increased temperature is greater than 85°. This is in contrast to the angle 206 of Figure 2. It is believed that the elevated temperature improves the wall angle by preferentially inhibiting polymer formation on the oxide sidewall as compared with the bottom of the opening. In some cases this provides a steep wall angle and an increase in selectivity. It has been found that the profile control is maintained even through layers of different types of oxide, such as doped and undoped, as well as various doping levels. In general, it is believed that the increased temperature causes all types of oxides to be less "sticky" than other layers, particularly nitride, so that high etch selectivity of oxide to silicon, silicon nitride, titanium silicide, etc. may be achieved. Further, the use of a higher temperature to improve wall profile without selectivity tradeoff is applicable to any process using any chemistry. Because the selectivity is improved or remains the same, at the higher temperature a greater process latitude results. For example, selective etches of relatively thick layers of BPSG, with good profile control may be achieved. Furthermore, the temperature increase generally increases the etch rate, so that throughput is higher. In addition to this improved wall angle, the embodiment illustrated in Figure 9 also achieves the earlier described advantages of the hard mask layer.

In the present invention it has been found that by the addition of Freon 134a to any etch chemistry, improved oxide:nitride selectivity is achieved, even in chemistries that do not otherwise exhibit oxide:nitride selectivity. Freon 134a has the formula $C_2H_2F_4$. An illustration of the Freon 134a molecule 1002 is shown in Figure 10A. In a currently preferred embodiment, the etch is performed in a mixture comprising Freon 134a, and Freon 23 (CHF_3). In one embodiment, the etch is performed with a Freon 134a flow rate of approximately 1.5 SCCM, a CHF_3 flow rate of approximately 47 SCCM, a pressure in the range of approximately 10 - 40 mTorr, a power of approximately 400 - 1200 W, and a DC bias in the range of approximately 1000 - 2000 V. Referring to Figure 11, oxide layer 1101 overlying nitride layer 1102 on substrate 1100 is shown. Substrate 1100 is generally similar to the substrates described previously, and oxide layer 1101 is generally similar to oxide layer 501. Hard mask layer 1105 has been patterned and etched to form an opening 1111 therein. An etch is performed as described above, and opening 1121 is shown during the etch process. As can be seen, the oxide sidewalls 1130 have minimal polymer deposition, while the bottom 1107 has some polymer buildup.

Although the precise mechanism is not known, it is believed that the Freon 134a of the present invention allows for such improved selectivity by working in combination with the polysilicon hard mask to reduce free fluorine (F) neutrals and ions, to reduce their concentration in the plasma, thus decreasing the F/C ratio at nitride surfaces as compared to oxide surfaces. This brings the etch into the regime where oxide etching is still at an acceptable rate, while little etching occurs on the nitride. It is further believed that the increased selectivity may result from the presence of a three carbon chain molecule formed by reaction with Freon 134a molecule 1002 with carbon from another source. It is believed that the Freon 134a undergoes the reaction shown in Figure 10B to create the stabilized molecule 1005. The molecule 1005 may then undergo a reaction with, for example, CHF_3 to form the above mentioned three carbon molecule. The improved selectivity has been found using Freon 134a together with, for example, CHF_3. However, it has been found that mixtures of CHF_3 and CH_2F_2 (Freon 32), mixtures of CHF_3 and CHF_2CF_3 (Freon 125), and mixtures of CHF_3 and C_2F_6 (Freon 116) do not exhibit the improved selectivity of Freon 134a, so that it appears the second hydrogen atom on the first carbon atom may be important to the proposed mechanism.

The improved selectivity of the present invention additionally is believed to be achieved in part by the F gettering action of the hard mask. Therefore, the hard mask 1105 is preferably polysilicon, or some other F reactive film such as silicon nitride, tungsten (W), titanium silicide (TiSi), etc. Of course, as with hard mask 505, hard mask 1105 is additionally preferably a non-carbon or very low carbon content film. The addition of Freon 134a has been found to work on a wide variety of different feature sizes, can be employed in a variety of processes and etch tools. Further, the improved selectivity can be achieved with minimal or no tradeoff with other performance goals. Additionally, the selectivity provided by the

present invention can be achieved without resort to processes having unstable plasma conditions and without resort to high polymer chemistries, thus avoiding the problems of difficult reactor maintenance, particle generation, and reduced wall profile control. For an existing etch process chemistry, varying amounts of Freon 134a may be added, depending upon the particular situation. For example, typically, Freon 134a may be added such that the Freon 134a flow is in the range of approximately 3 - 50% of the total flow.

It will be appreciated that in many prior art processes with high selectivity, in addition to the wall profile control problem, it is often difficult to completely etch the oxide layer, especially in deep openings. However in the present invention, since the carbon contribution from the photoresist is removed, the selectivity is achieved without the problem of excessive polymer buildup in the bottom, so that openings may be etched to completion. Additionally, in the present invention, it has been found that due to the sticking of polymer to nitride, nearly infinite selectivity to nitride is achieved. That is, after a small initial amount is etched, polymer buildup begins so that regardless of the length of the etch, nitride etching does not continue after the small initial amount is etched.

As discussed in relation to Figure 4, in addition to the difficulty in achieving oxide:nitride selectivity, it is further difficult to achieve nitride uniformity within the bottom of the contact and to avoid removing the nitride etch stop layer from the structure 404. Figures 12 - 14 illustrate a further embodiment of the present invention overcoming this problem. Referring to Figure 12, hard mask layer 1205 is formed on oxide layer 1201. In one embodiment, oxide layer 1201 comprises a 2000 Å undoped TEOS layer on top of a 12000 Å BPSG layer. The hard mask 1205 is preferably polysilicon or another F gettering material as described in relation to hard mask 1105. Photoresist layer 1210 has opening layer 1211 which is aligned to form an opening in the oxide which will partially overlie the structure 1204, i.e., the etch must extend over a corner. For example, the process step illustrated in Figure 12 may be a self-aligned contact etch. Referring now to Figure 13, hard mask 1205 is etched in the region exposed by opening 1211, to form opening 1216. After forming opening 1216, photoresist layer 1210 is removed.

In a currently preferred embodiment, an oxide etch is performed through hard mask 1205, utilizing a gas chemistry comprising Freon 134a at high temperature. In a currently preferred embodiment, the etch is performed in a flow comprising 10 SCCM CHF_3 and 2.5 SCCM Freon 134a, at a power of 600 W. The backside helium pressure is 2 Torr. As described previously, the use of Freon 134a together with the hard mask 1205 increases the oxide:nitride selectivity. The use of increased wafer temperature provides good wall profile control and provides further improvement in the oxide:nitride selectivity, leading to good nitride layer uniformity on both horizontal and vertical surfaces. Hard mask 1205, in addition to improving selectivity also provides reduced ARDE effects. As can be seen in Figure 14, opening 1221 is formed in oxide layer 1201, while a uniform portion of nitride layer 1203 remains on structure 1204 and a uniform portion of nitride layer 1202 remains on the bottom portion 1230 of the opening 1221. It will be appreciated that the nitride layers 1202 and 1203 may or may not be formed in the same processing step. In one embodiment, nitride layer 1202 and 1203 have a thickness of approximately 700 Å. With the above described etch characteristics, the present invention provides improved results for structures such as that shown in Figures 12 - 14. Because the present invention achieves the high oxide:nitride selectivity described above, the problems described in relation to Figure 4, over a corner of a structure, do not occur. Additionally, since nitride uniformity is maintained over both corners and flat surfaces, the present invention can be used to perform an oxide etch wherein there are openings that overlie corners and openings that overlie flat surfaces. Additionally, since hard mask 1205 minimizes the ARDE effect, the openings may have different aspect ratios from one another. Note that these results are achieved with existing reactor technology, and without requiring substantial reengineering of the etch process. The present invention provides for an improved process window for an etch over topography and flat surfaces, and of course provides greater process latitude in any type of etch.

A further embodiment of the present invention allows for increased etch depth to be achieved without sacrificing etch performance. Referring to Figure 15, patterning layer 1510 having openings 1511 and 1512 is formed on hard mask layer 1505 which has been deposited on oxide layer 1501. Oxide layer 1501 may be a relatively thick oxide having a depth in the range approximately 5,000 - 30,000 Å. Oxide layer 1501 may comprise several layers of one or more different types of oxide layers. For example, in one embodiment oxide layer 1501 may comprise an uppermost CVD TEOS oxide layer of approximately 3,000 Å, overlying one or more BPSG layers with a total thickness of approximately 10,000 Å - 20,000 Å. Typically, it is difficult to etch through such a thick layer completely due to polymer buildup in the bottom of the forming opening. Further, for the reasons described previously, it is difficult to maintain the etch wherein the openings have different aspect ratios, and wherein some openings may be overlying structures.

Therefore, in a further embodiment of the present invention, an etch is performed through hard mask layer 1505 to form openings 1516 and 1517 shown in Figure 15. Next, with resist layer 1510 in place, a high etch rate oxide etch is performed which is preferably designed to etch one or more layers of the uppermost portion of oxide layer 1501. For example, in one embodiment the etch is tailored to etch the undoped layer and some of the doped layer. In one embodiment the etch is performed in a flow comprising 70 SCCM CHF_3 and 20 SCCM C_2F_6 (Freon 116). The etch is performed at a power of 600 W, and a

pressure of 50 mTorr. A h lium coolant pressure of 8 Torr is used, and the lower electrode water coolant temperature is set a 17° C. Next, a polymer removal step is performed. The polymer may be ashed in an oxygen plasma, for example, or a wet chemical etch may be p r-formed. For example, in one embodiment a first clean step in an IPC barrel ash system, performed in a flow of oxygen (O_2) at 1.5 Torr, 400 W for 45 minutes is performed followed by a clean in a solution of $H_2SO_4 \cdot H_2O_2$ at 150° C for 20 minutes. It will be appreciated that if desired, the polymer clean may be performed using a single step, similar to one of the above described steps. Additionally, it will be appreciated that many similar clean steps may be performed. During the polymer removal step, the patterning layer 1510 is also removed.

Figure 16 shows the structure of Figure 15 after these steps have been performed, and partial openings 1521' and 1522' have been formed. As can be seen, a substantial thickness of oxide layer 1501 has been removed. Additionally, all polymer has been removed from the openings. Next, one of the above described etches of the present invention, such as that described in conjunction with Figures 12 - 14, comprising Freon 134a, and at high temperature is performed. The structure of Figure 16 after the second etch step is shown in Figure 17. As shown, openings 1521 and 1522 extend all the way through oxide layer 1501 to the surface of nitride layer 1502, which remains uniform in the bottom of the opening. Additionally, nitride layer 1503 overlying structure 1504 remains intact. As described above, the temperature of the etch can be varied for the desired taper. For example, an angle 1506 of 85° - 90° can be achieved by reducing the helium flow and pressure such that the wafer temperature is elevated as described before. Alternatively, normal cooling can be performed so that the angle 1706 has a taper of less than 85° if desired.

As described earlier, use of a hard mask during the oxide etch process eliminates the interaction of the photoresist with the etch chemistry. By forming a structure such as that shown in Figure 13, a variety of etch chemistries and conditions may be explored to determine polymer formation under these conditions and in the absence of interference from the photoresist. For example, under certain conditions, polymer deposition was found to occur on the top, horizontal surface of a hard mask such as hard mask 1205 during the etch process. In the prior art, although polymer deposition on the sidewalls, nitride surfaces within openings, and the bottoms of trenches has been known, deposition on an upper surface, such as the upper surface of layer 1205 of Figure 13 has not been known. This is due to the fact that the upper horizontal surface receives sufficient ion bombardment to prevent polymer formation. In contrast, opening sidewalls and structures in sidewalls receive significantly less ion bombardment.

Therefore, in a further embodiment of the present invention, a photoresist mask is used under conditions causing formation of the polymer film on the upper surfaces of the hard mask. Referring to Figure 18, substrate 1800 having structure 1804, nitride layer 1802, and oxide layer 1801 is shown. In general, these layers and structures are similar to those described in conjunction with Figure 12, for example, or may be similar to layers or structures described in conjunction with other embodiments of the present invention. A photosensitive layer, such as positive photoresist layer 1810 is formed thereon, having a thickness in the range of approximately 1.0 - 1.5 microns in one embodiment. Photoresist layer 1810 comprises opening 1811, formed by well known methods. Photoresist layer 1810 may be used as a mask to form a contact opening or via in the oxide layer 1801 in the region exposed by opening 1811.

In a currently preferred embodiment, the etch is carried out in a LAM 384T dry etch system. In a system designed for 8 inch wafers, the etch is carried out in a flow comprising approximately 3 SCCM Freon 134a and 10 SCCM CHF_3. The etch is carried out at a power in the range of approximately 300 - 400 W, and preferably approximately 350 W, with a DC bias of approximately 1200 volts. In one embodiment, the etch is performed at a pressure in the range of approximately 20 - 50 mTorr, and preferably approximately 35 mTorr. Also in a currently preferred embodiment, the helium pressure is approximately 1.5 Torr, which typically results in a helium flow in the range of approximately 1 - 2 SCCM. With this helium flow, the wafer can be expected to reach temperatures of approximately 90°. This temperature is below the temperature used in some embodiments of the present invention, using a hard mask, since the temperature must be maintained at approximately no higher than the resist reticulation temperature.

Furthermore, several modifications were made to the system. For example, in this system, a grid structure made of, for example, aluminum, having a plurality of openings therein, is disposed between the upper and lower electrodes. This grid may have a voltage applied thereto or may, as in one embodiment, be grounded during the etch. A typical opening size in the grid is approximately 9 mm. However, in one embodiment an opening size of approximately 15 mm is used. The use of larger openings decreases the dark space, and results in a more intense plasma. Further, in one embodiment, the electrode spacing was in the range of approximately 1.3 - 1.8 inches, and preferably approximately 1.6 inch. This spacing is greater than a typical prior art spacing of approximately 0.6 inch. Finally, in one embodiment, the standard roots blower mechanical pump was replaced with a turbo pump, and the pumping lines were changed from 2 inch to 3 inch to allow for greater pumping speed. These modifications typically allow for a greater (for example, approximately 4 times as great) gas flow at a given pressure.

Referring now to Figure 19, the substrate of Figure 18 is shown after the beginning of the above-described etch process. As shown, a thin layer 1901 of polymer has formed on the upper surface of resist layer 1810, as well as the sidewalls of opening 1811. This polymer deposi-

tion essentially encapsulates the resist layer, such that resist/plasma interaction is eliminated. With this encapsulation, an essentially infinite oxide resist etch rate is achieved, so that the resist mask remains intact for the duration of the etch. Although the upper surface of the resist layer 1810 receives polymer deposition, etching of the oxide layer 1801 in the region exposed by opening 1811 continues to occur. It is believed that polymer deposition occurs on the surface of resist layer 1810 due to an increased neutral:charged ion ratio in the plasma of the present invention, as well as other factors resulting in polymer formation/sticking at the surface of resist layer 1810. Although these conditions have been found to lead to polymer deposition on surfaces of layers such as resist layer 1810, or a hard mask made of, for example, polysilicon, an oxide layer does not see a net polymer deposition, even in the presence of a high neutral flux, due to the reactivity of the oxide layer in the presence of ion bombardment, as compared with these other layers.

Typically, in the prior, as described above, while polymer formation on the sidewalls of opening 1811 may occur, polymer deposition on the upper surface of a resist layer does not occur. Because of this, the resist etches at some finite rate in the prior art due to the ion bombardment. Further, the corners typically pull back slightly as the resist layer is etched. For example, dashed lines 1905 illustrate the etching of photoresist layer 1810, near the opening in a prior art process. Eventually, as the etch proceeds, this pulling back of the corners may result in an excessively tapered opening. In contrast, in the present invention, the resist profile maintains intact due to the polymer layer 1901 present on the upper surface of layer 1810 as well as the sidewalls of opening 1811. Additionally, because the resist remains intact, etches through relatively thick oxide layers may be performed.

Referring to Figure 20, the substrate of Figure 19 is shown at the completion of the etch. As shown, polymer layer 1901, in addition to encapsulating photosensitive layer 1810, also adheres to nitride layer 1802, and oxide sidewall 1801. The sidewall polymer buildup is typically partially due to the fact that the sidewalls receive less ion bombardment as described above. Also as described earlier, the amount of polymer on an oxide sidewall such as sidewall 1801 will be dependent upon process conditions, especially temperature and etch chemistry. In a preferred embodiment, although the polymer layer 1901 forms on the sidewall 1801, the temperature of the above-described embodiment is sufficiently high such that an acceptable wall angle is obtained. Additionally, as described earlier, the etch chemistry leads to preferential buildup on nitride surfaces, giving good oxide:nitride selectivity. With the formation of polymer layer 1901 on nitride layer 1802, no etching of the nitride layer 1802 occurs on top or side surfaces, so that the corner of structure 1804 remains intact. Therefore, as with other embodiments of the present invention, high selectivity, even over corners of structures, and in long etches through thick oxide layers, may be maintained.

The use of the process described in conjunction with Figures 18 - 20 is advantageous in that it eliminates the deposition and etch of a hard mask, and eliminates the removal of photoresist, and any clean steps in the earlier described hard mask embodiments. Thus, use of the polymer deposition mode provides many of the advantages of the hard mask embodiments in a less costly and complex process.

As described above, the polymer deposition mode was found by initially utilizing a hard mask embodiment without photoresist. In this way, the polymer deposition properties, absent interactions with the resist, can be determined. Once a set of conditions is found that results in polymer deposition on upper, horizontal surfaces, that set of conditions may be used in an embodiment having a photoresist mask, since the polymer deposition will quickly eliminate resist/plasma interaction. It will be appreciated that while the earlier described etch parameters provide for the encapsulated resist layer, other process conditions may be utilized, in accordance with the guidelines described below, which result in the encapsulation of resist, leading to the benefits of the present invention, including reduced or eliminated aspect ratio dependency effects.

By forming a structure such as that shown in Figure 13, one of skill in the art may adjust the chemistry, power, time, and equipment configuration, to suit the particular equipment and process step of interest. For example, as mentioned above, in one embodiment the openings in the grid were increased. This provides for a more efficient plasma, leading to more non-charged chemical species in the plasma. This results in a plasma that is more likely to deposit polymer on the resist layer 1810 surface than a plasma with a higher flux of ions, which is more likely to cause etching of the resist. Further, the increase in the electrode spacing, by making the wafer slightly more distant from the plasma discharge, has the same effect by decreasing the ion flux at the resist surface. Thus, one of skill in the art may use these considerations to make adjustment to the equipment if desired, to achieve a plasma that deposits a polymer on the resist layer while etching the oxide layer. Additionally, adjustments to the etch chemistry or other process parameters, in addition to or instead of modification to the equipment may be made. For example, increasing the concentration of one or more etchants such as Freon 134a, CHF_3, H_2, which are known to lead to increased polymer formation may be used.

As described above, an acceptable set of conditions may be determined on an embodiment wherein a hard mask, without a resist layer, is used. In this regard, some minor adjustment has been made to the hard mask embodiment used to characterize the process compared with the conditions described in relation to the embodiment of Figures 18 - 20. For example, the embodiment with resist layer 1810 was carried out at a pressure of approximately 5 mTorr greater than the process as characterized on the hard mask embodiment. Additionally, the temperature of the resist embodiment of Figures 18

- 20 is slightly lower than the hard mask characterization process. In general, these changes are made to increase the neutral ion flux in th opening, to maintain polymer buildup therein, since th photoresist layer is approximately 5 times or more thicker than the hard mask layer. The pressure increase increases the overall polymer flux, while the temperature decrease increases sidewall sticking. Of course, as mentioned earlier, the temperature should be no higher than the resist reticulation temperature. Although, as mentioned above, the system of the preferred embodiment was modified to increase gas flow, such a modification will typically not be necessary, as a normal mechanical pump appears to provide sufficient pump speed.

Thus, a method of etching an oxide layer has been described. Although specific embodiments, including specific equipment, parameters, methods, and materials have been described, various modifications to the disclosed embodiments will be apparent to one of ordinary skill in the art upon reading this disclosure. Therefore, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention and that this invention is not limited to the specific embodiments shown and described.

Claims

1. A method of etching an oxide layer comprising:
providing a substrate having said oxide layer thereon:
forming a photosensitive layer on said oxide layer;
forming a first opening in said photosensitive layer to expose a portion of said oxide layer;
exposing said substrate to a plasma, said plasma etching said exposed portion of said oxide layer and forming a first layer on said photosensitive layer.

2. The method as described in claim 1 wherein said first layer comprises a polymer.

3. The method as described in claim 1 wherein said plasma is formed in a flow comprising Freon 134a.

4. The method as described in claim 3 wherein said flow further comprises CHF_3.

5. The method as described in claim 1 wherein said plasma is formed using an RF power in the range of approximately 300 - 400 W.

6. The method as described in claim 1 wherein said plasma is formed between two electrodes having a spacing in the range of approximately 1.3 - 1.8 inches.

7. The method as described in claim 3 wherein said plasma is formed between two electrodes having a spacing in the range of approximately 1.3 - 1.8 inches.

8. The method as described in claim 1 wherein said oxide layer opening exposes a corner of a structure.

9. The method as described in claim 3 wherein said oxide layer opening exposes a corner of a structure.

10. The method as described in claim 6 wherein said oxide layer opening exposes a corner of a structure.

11. The method as described in claim 8 wherein said substrate comprises a nitride layer underlying said oxide layer, said nitride layer disposed on said corner.

12. The method as described in claim 1 wherein said photosensitive layer is the uppermost layer on said substrate prior to said formation of said first layer, and wherein at least a portion of said photosensitive layer having said first layer formed thereon is substantially parallel to a surface of said substrate.

13. The method as described in claim 3 wherein said photosensitive layer is the uppermost layer on said substrate prior to said formation of said first layer, and wherein at least a portion of said photosensitive layer having said first layer formed thereon is substantially parallel to a surface of said substrate.

14. The method as described in claim 6 wherein said photosensitive layer is the uppermost layer on said substrate prior to said formation of said first layer, and wherein at least a portion of said photosensitive layer having said first layer formed thereon is substantially parallel to a surface of said substrate.

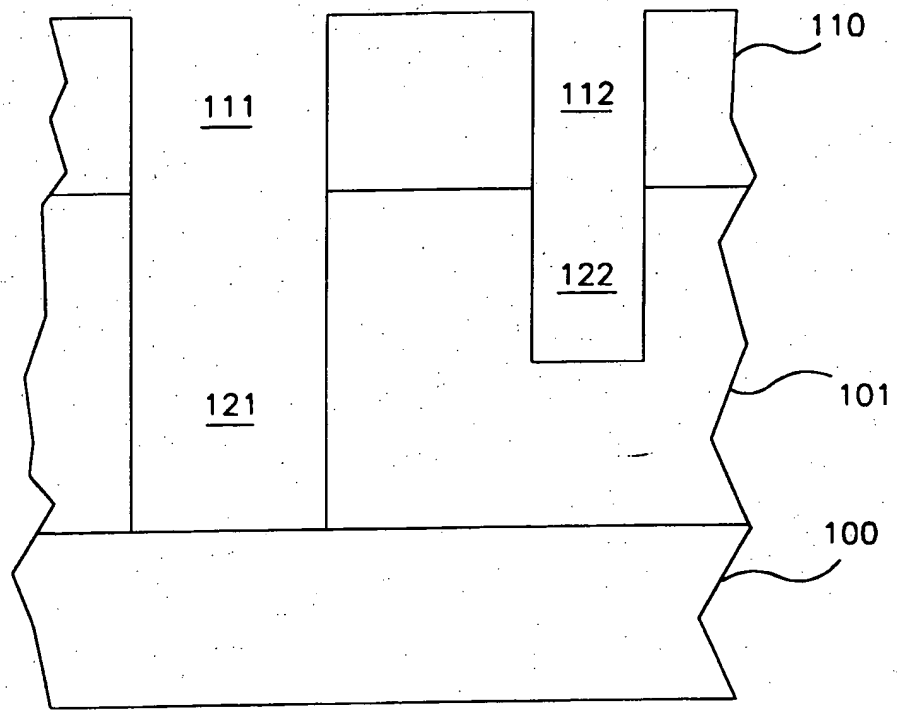

FIG. 1
(PRIOR ART)

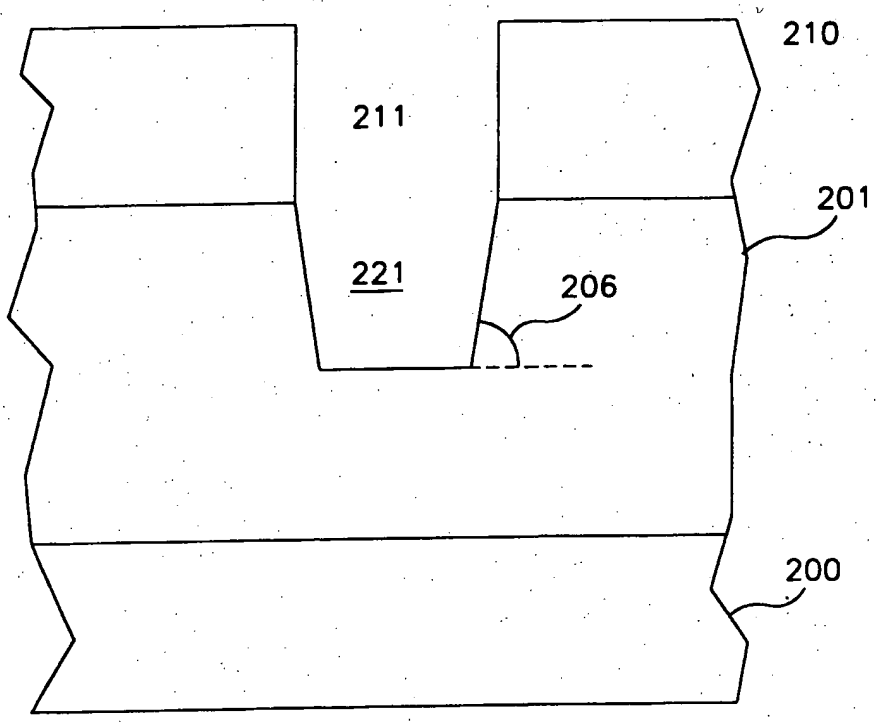

FIG. 2
(PRIOR ART)

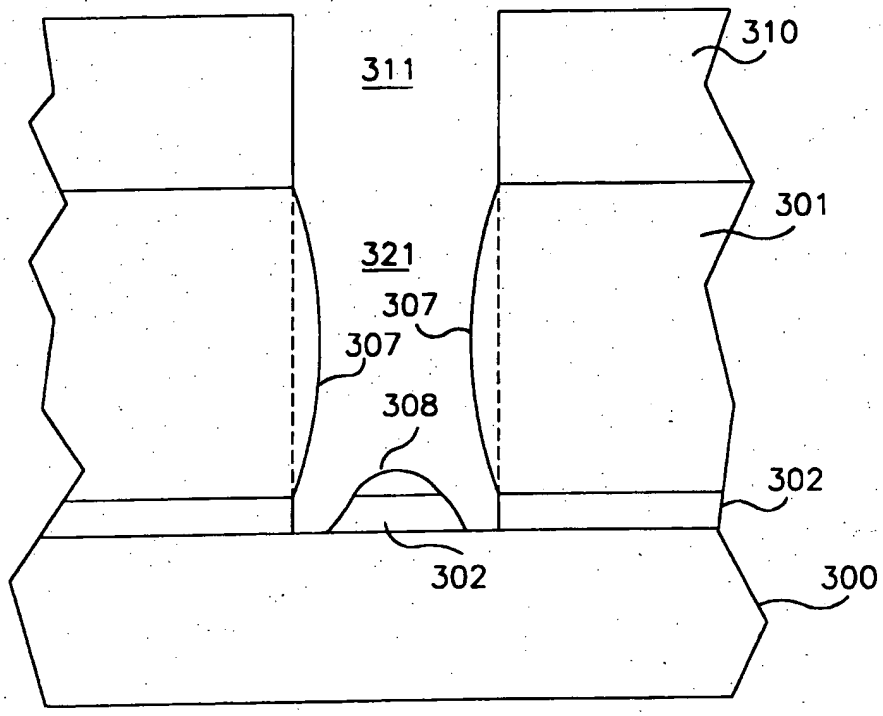

FIG. 3
(PRIOR ART)

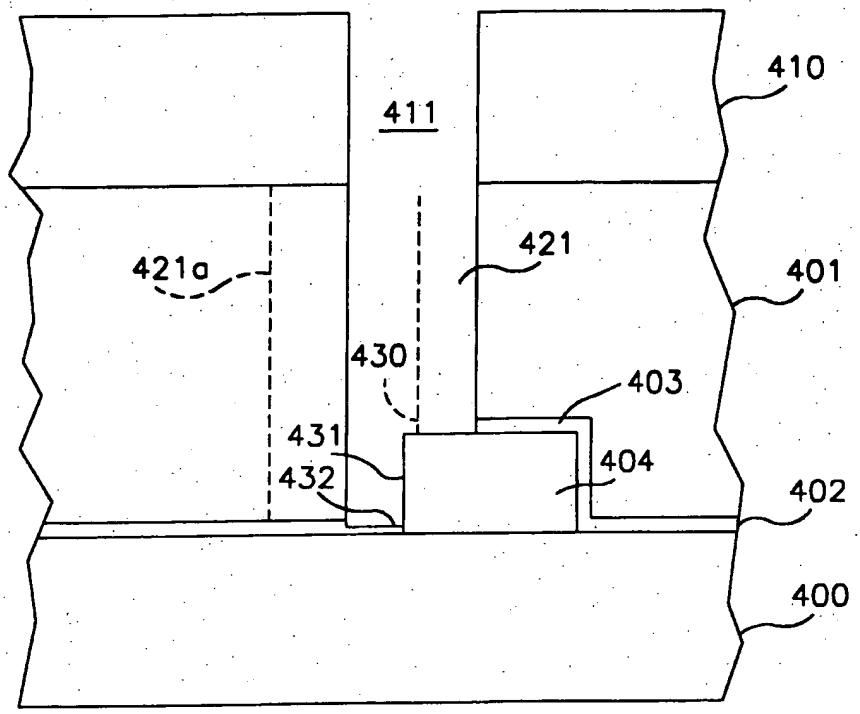

FIG. 4
(PRIOR ART)

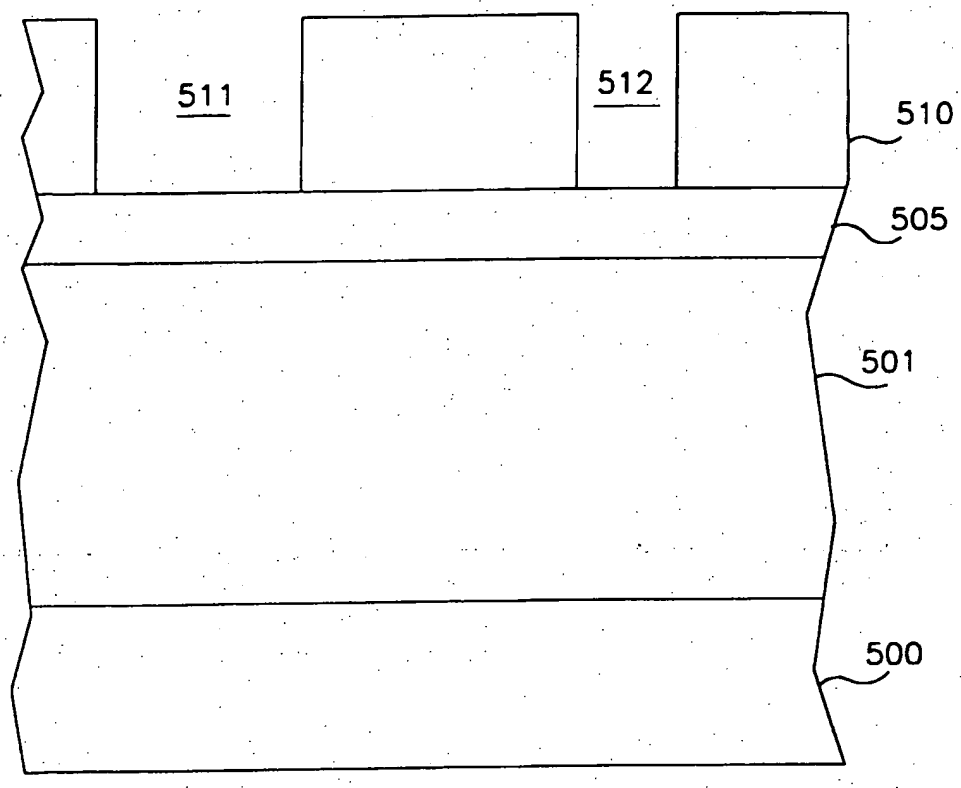

FIG. 5

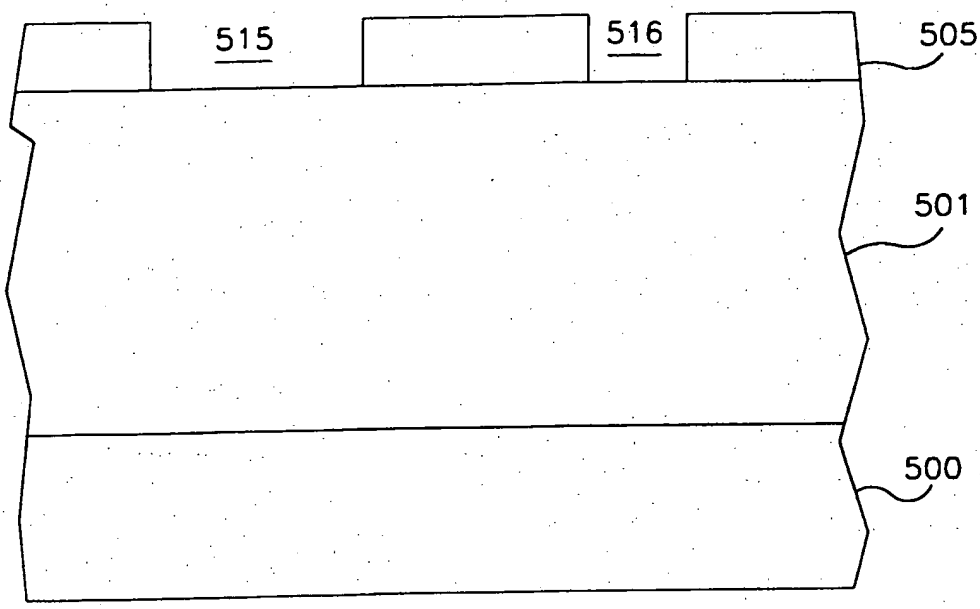

FIG. 6

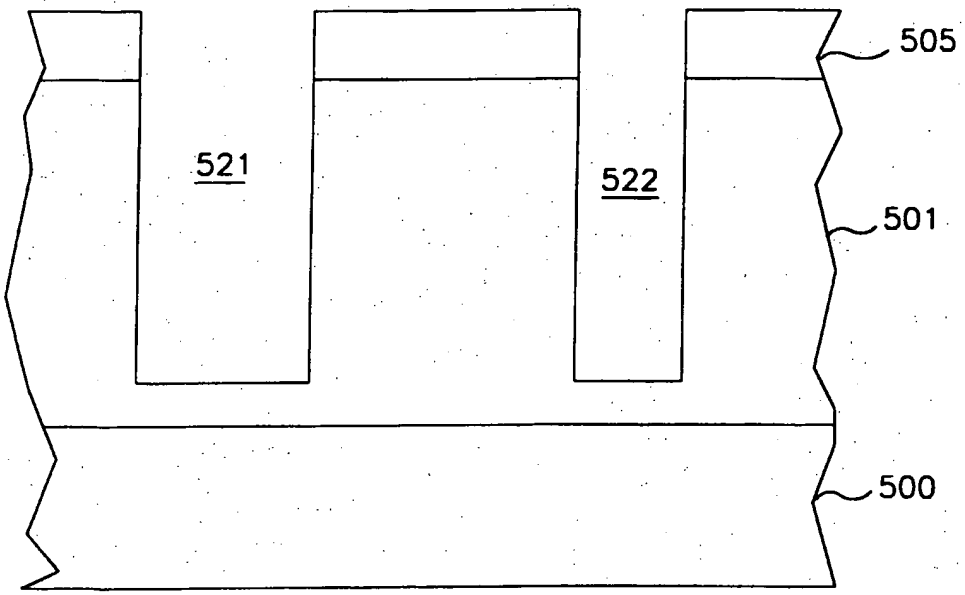

FIG. 7

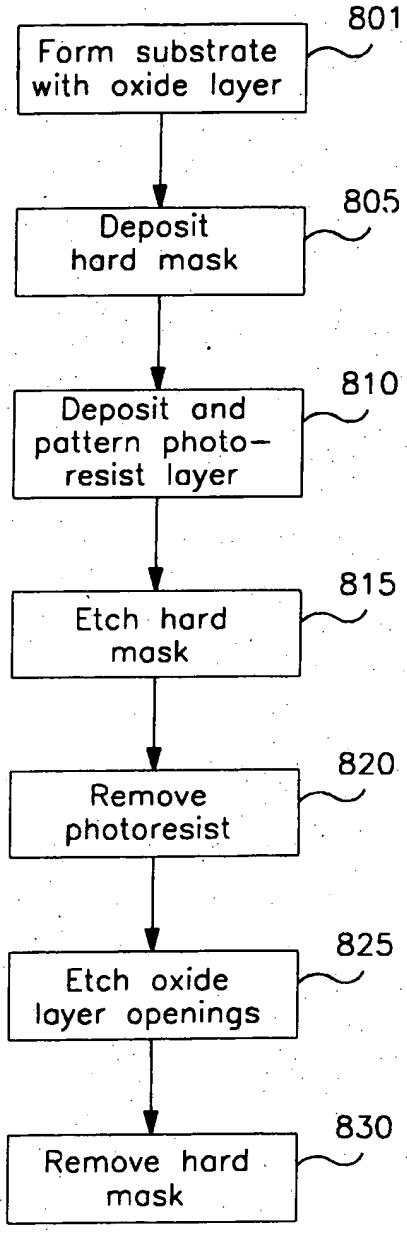
801
Form substrate with oxide layer
805
Deposit hard mask
810
Deposit and pattern photo-resist layer
815
Etch hard mask
820
Remove photoresist
825
Etch oxide layer openings
830
Remove hard mask

FIG. 8

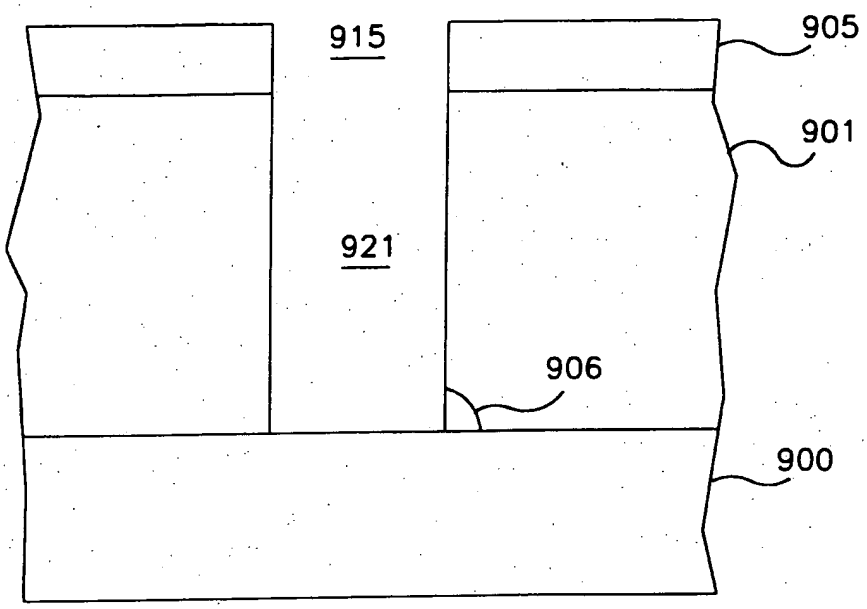

FIG. 9

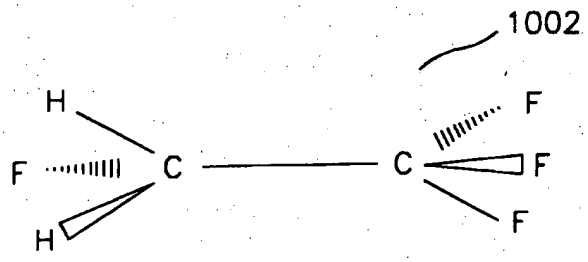

FIG. 10A

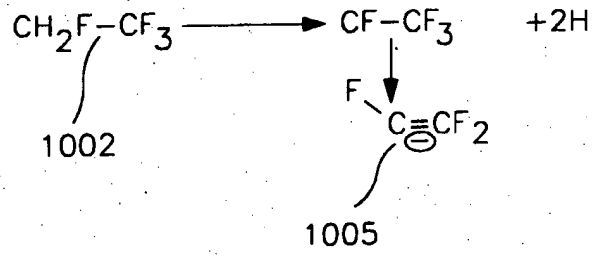

FIG. 10B

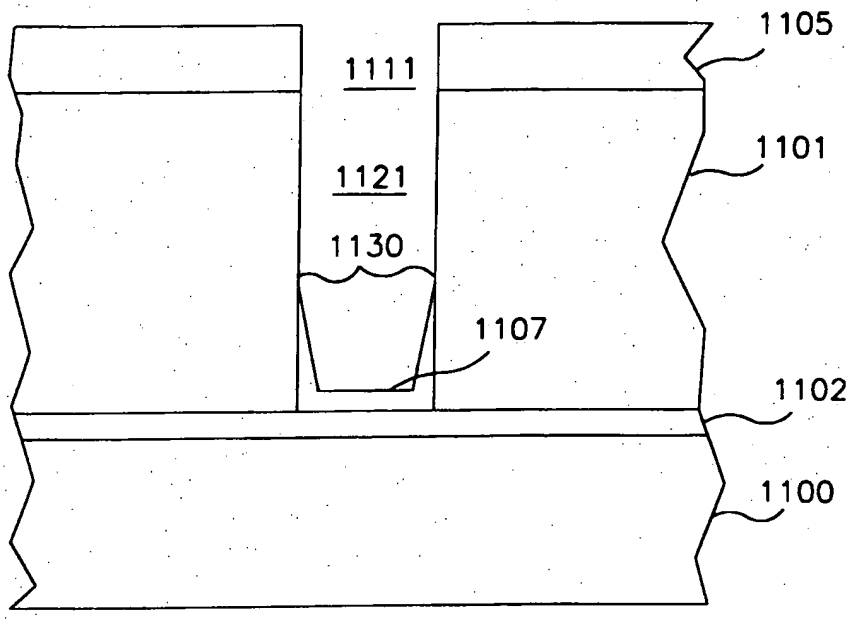

FIG. 11

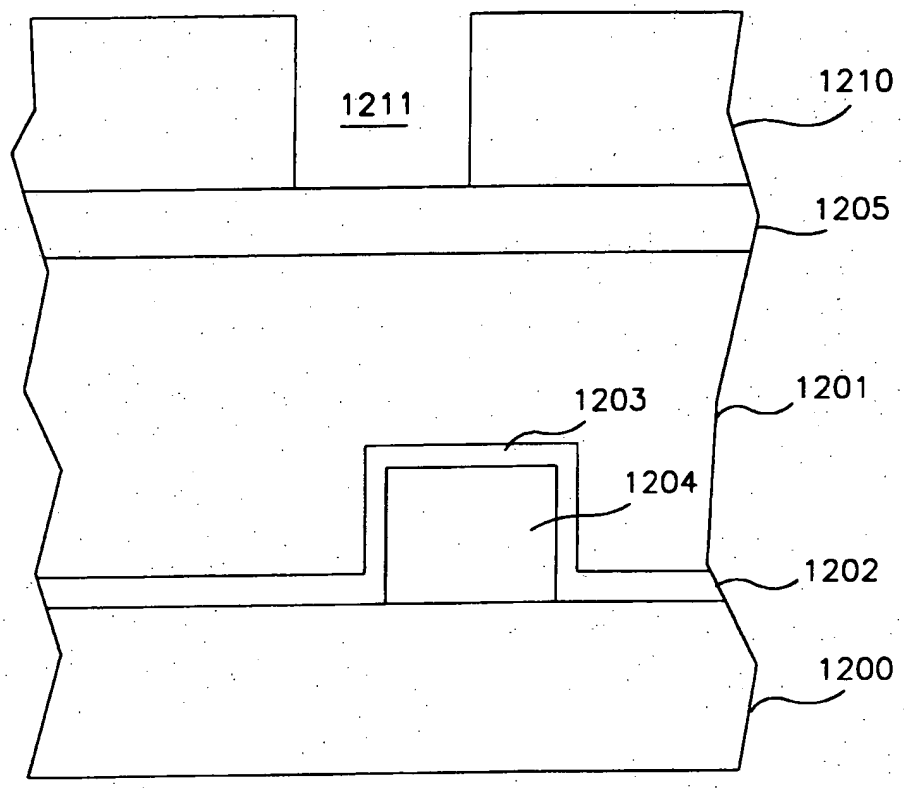

FIG. 12

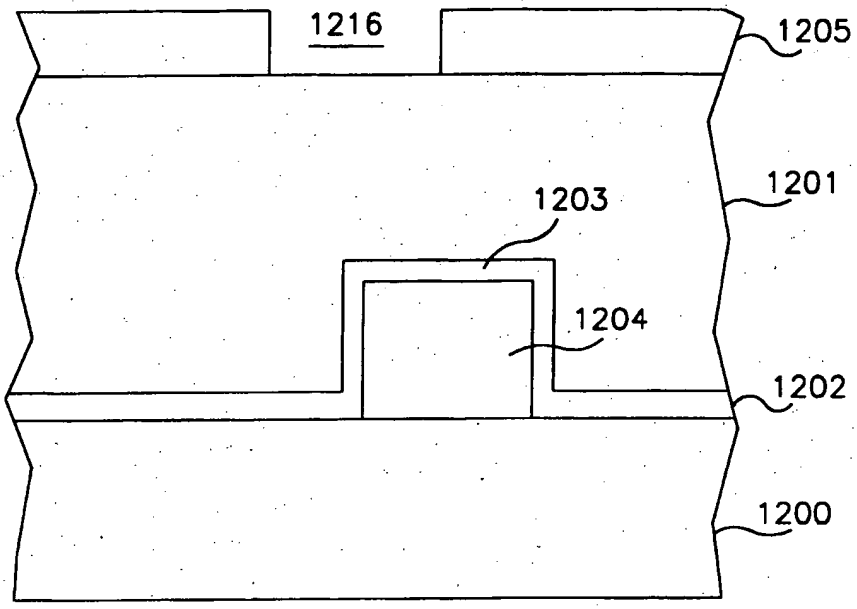

FIG. 13

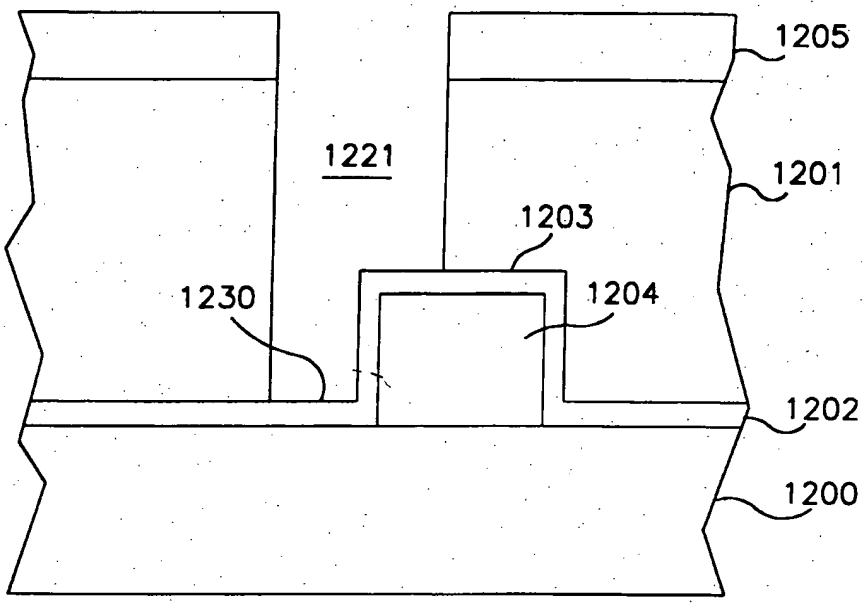

FIG. 14

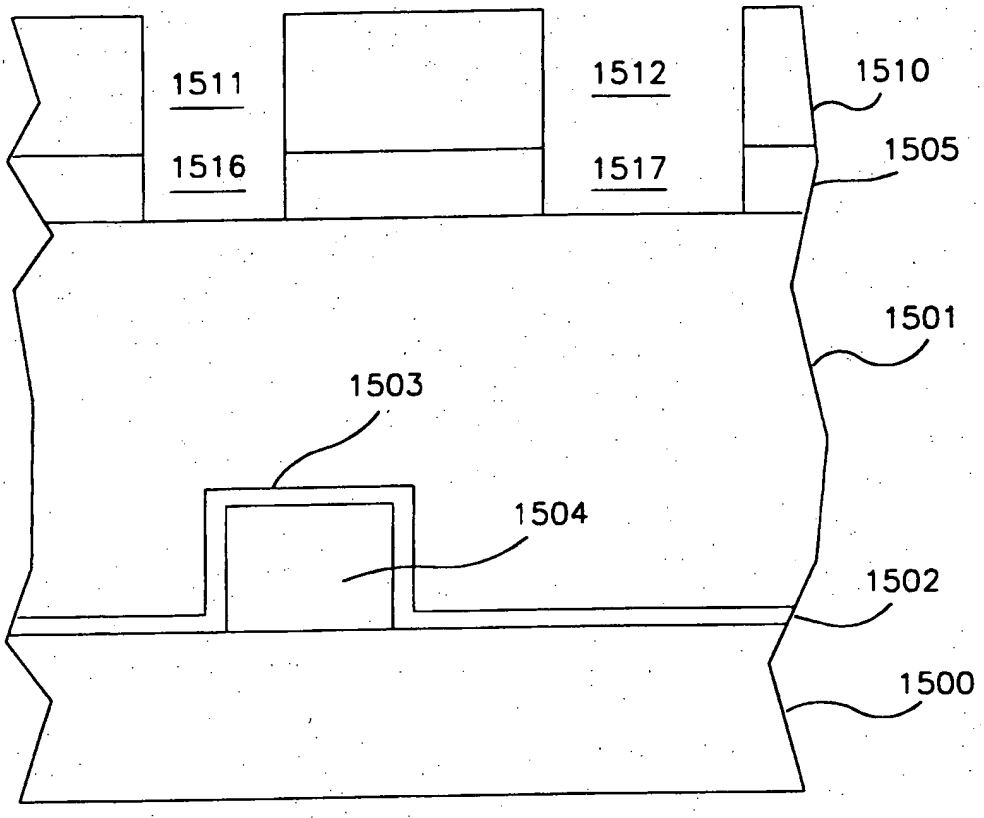

FIG. 15

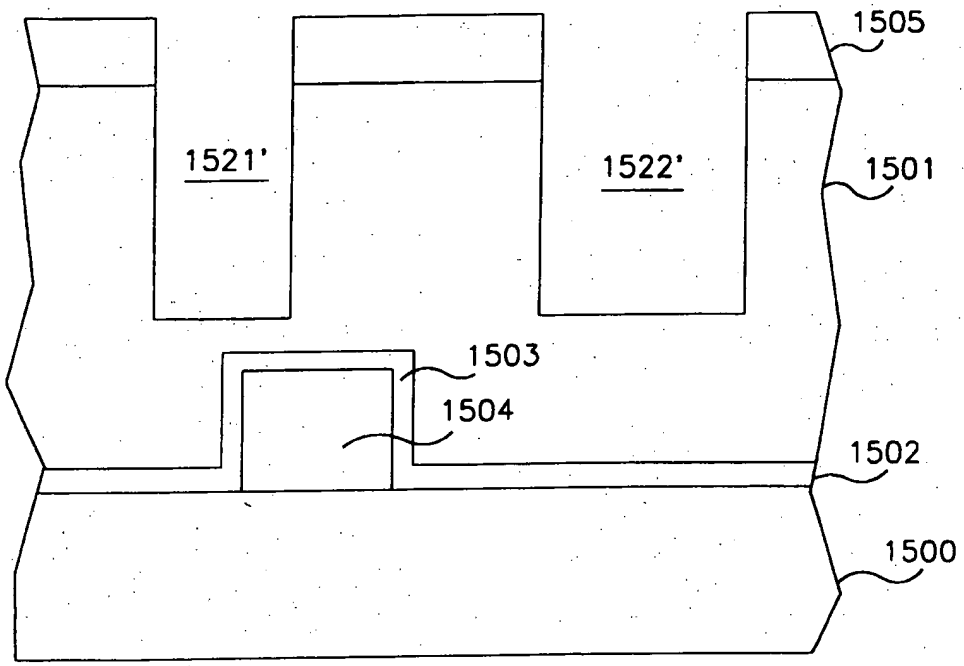

FIG. 16

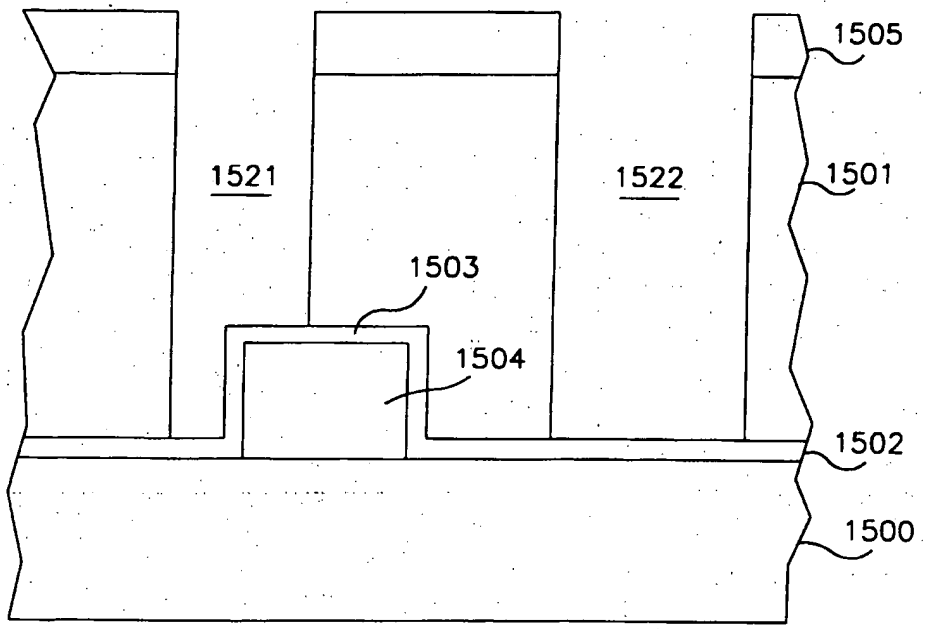

FIG. 17

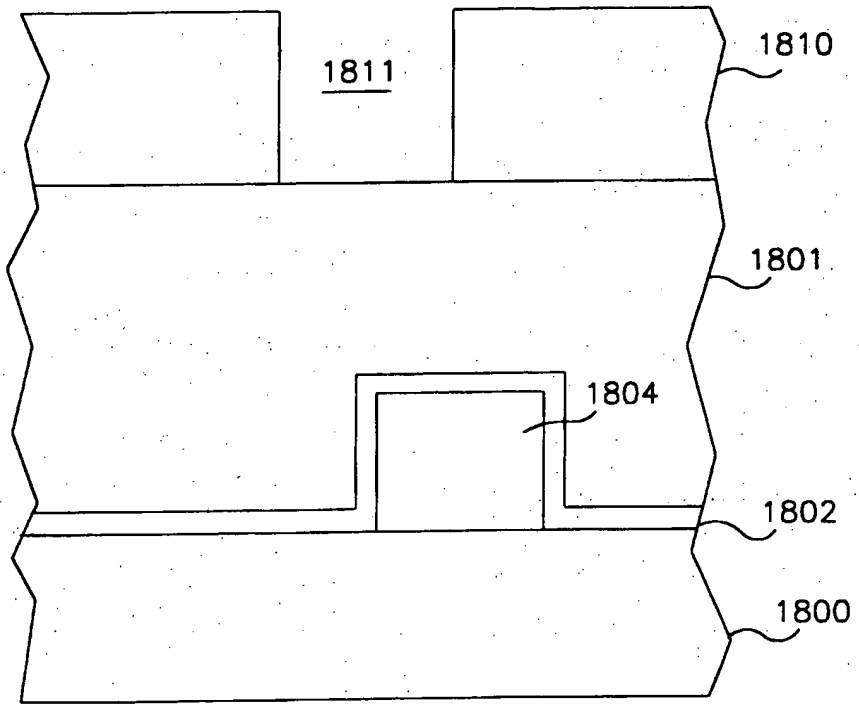

FIG. 18

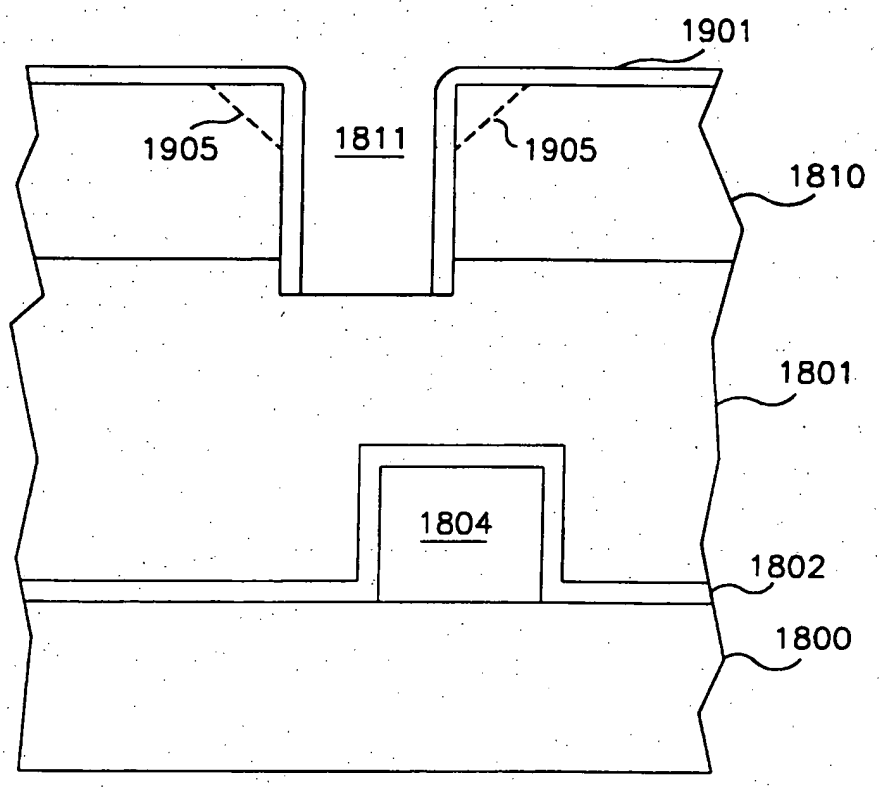

FIG. 19

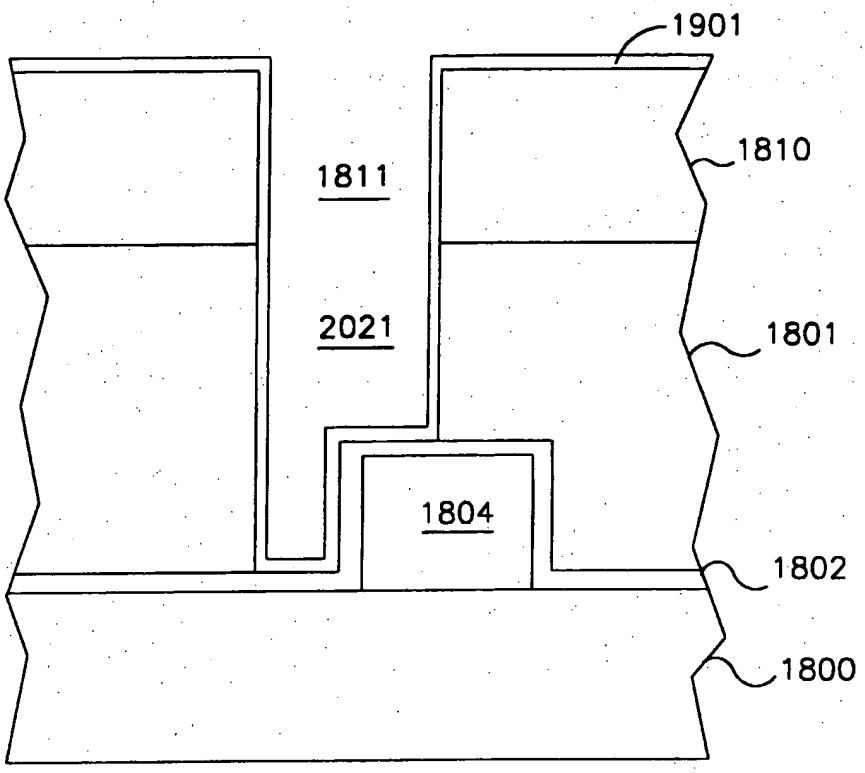

FIG. 20

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European Patent Office
Office européen des brevets

(11) EP 0 721 205 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
10.12.1997 Bulletin 1997/50

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(51) Int. Cl.[6]: **H01L 21/311**, H01L 21/768

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DE FR GB IT

(30) Priority: **07.12.1994 US 351784**

(71) Applicant:
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San Jose, California 95128 (US)

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15, Hamilton Square
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(54) Method of etching an oxide layer with simultaneous deposition of a polymer layer

(57) A method of etching an oxide layer is disclosed. First, a resist layer is formed on an oxide layer on a substrate. Next, a photosensitive layer is formed on the oxide layer and patterned to expose regions of the oxide layer to be removed. The exposed regions may overlie a nitride layer, and may overlie a structure such as a polysilicon gate. The etch is performed such that polymer deposits on the photosensitive layer, thus eliminating interactions between the photosensitive layer and the plasma. In this way, a simple etch process allows for good control of the etch, resulting in reduced aspect ratio dependent etch effects, high oxide:nitride selectivity, and good wall angle profile control.

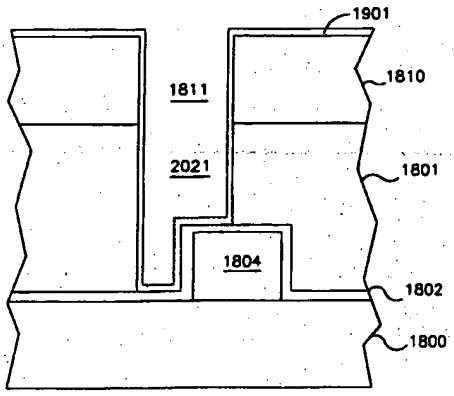

FIG. 20

EP 0 721 205 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 30 7589

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	GB 2 085 809 A (WESTERN ELECTRIC CO) 6 May 1982 * page 1, line 5 - line 8 * * page 1, line 23 - line 42 * * page 1, line 54 - line 68 * * page 2, line 12 - line 26; figure 3 * * page 2, line 81 - page 3, line 20; figure 4 * * page 3, line 41 - line 61 * * page 3, line 112 - line 119 *	1,2,12	H01L21/311 H01L21/768
Y		3-11,13, 14	

Y	EP 0 496 614 A (NIPPON ELECTRIC CO) 29 July 1992 * column 3, line 1 - column 4, line 27; figures 1A-1C *	3,4,7,9, 13	
A		1,2	

Y	US 5 246 882 A (HARTMANN JOEL) 21 September 1993 * column 5, line 45 - column 7, line 47; figures 3A-3E *	5,6,8, 10,11,14	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
A		1,2,4, 12,13	H01L

X	EP 0 516 053 A (SONY CORP) 2 December 1992 * column 1, line 1 - line 7 * * column 3, line 39 - column 4, line 17 * * column 5, line 1 - line 8 * * column 7, line 13 - column 8, line 44; figures 1A,1B *	1,12	
A		11	

	-/--		

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	24 September 1997	Klopfenstein, P

CATEGORY OF CITED DOCUMENTS

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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 30 7589

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
P,X	US 5 429 710 A (AKIBA HARI ET AL) 4 July 1995 * column 1, line 5 - line 11 * * column 5, line 57 - column 6, line 60; figures 2A-2C * ---	1,2,5,12	
E	EP 0 690 486 A (TEXAS INSTRUMENTS INC) 3 January 1996 * page 4, line 8 - line 27; figures 2A-2E * * page 4, line 48 - line 54 * -----	1,2	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	24 September 1997	Klopfenstein, P

CATEGORY OF CITED DOCUMENTS

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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

REMARKS

The Office Action dated September 22, 2003, has been received and reviewed.

Claims 1, 2, 4, 5, and 7-46 are currently pending and under consideration in the above-referenced application, each having been rejected.

The only claim amendments that are presented herein replace the term "said" with "the." As these are equivalent terms and the revisions have been made merely for formal purposes, these revisions do not alter the scope of any of the amended claims.

Reconsideration of the above-referenced application is respectfully requested.

Information Disclosure Statement

Please note that Information Disclosure Statements were filed in the above-referenced application on January 3, 2002, June 30, 2003, and September 8, 2003, but that undersigned attorney has not yet received any indication that the references cited in these Information Disclosure Statements have been considered. It is respectfully requested that the references cited in each of the Information Disclosure Statements be considered and made of record in the above-referenced application and that initialed copies of the Forms PTO-1449 that accompanied the Information Disclosure Statements be returned to the undersigned attorney as evidence of such consideration.

Rejections Under 35 U.S.C. § 112, First Paragraph

Claims 1, 2, 4, 5, and 7-46 stand rejected under 35 U.S.C. § 112, first paragraph, for purportedly failing to comply with the written description requirement.

Specifically, claims 1 and 20 have been rejected under the first paragraph of section 112 for including a negative limitation which was not expressly set forth in the specification of the above-referenced application. In rejecting claims 1 and 20, the Office cited *Ex Parte Parks,* 30 USPQ2d 1234, 1236 (Bd. Pat. App. & Inter. 1994), asserting that *Parks* requires that any exclusionary provision have basis in the original disclosure.

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 21/302

A1

(11) International Publication Number: WO 98/49719

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(22) International Filing Date: 16 February 1998 (16.02.98)

(30) Priority Data:
08/846,671 30 April 1997 (30.04.97) US

(71) Applicant: MICRON TECHNOLOGY, INC. [US/US]; 8000 South Federal Way, P.O. Box 6, Boise, ID 83707-0006 (US).

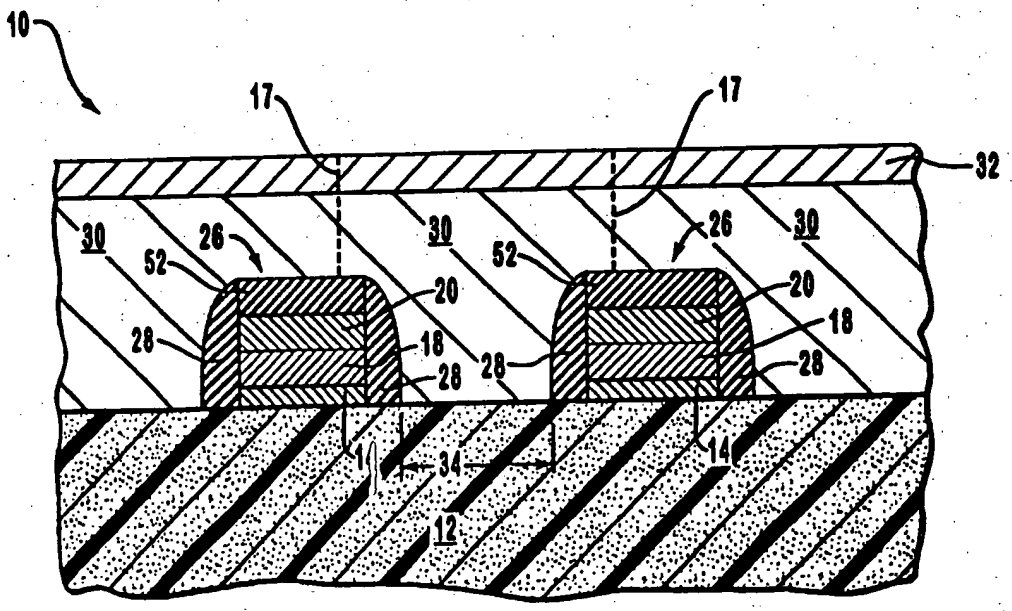
(72) Inventor: KO, Kei-Yu; 4611 East Rockbury Court, Meridian, ID 83642 (US).

(74) Agents: DESANDRO, Bradley, K. et al.; Workman, Nydegger & Seeley, 1000 Eagle Gate, 60 East South Temple, Salt Lake City, UT 84111 (US).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: UNDOPED SILICON DIOXIDE AS ETCH STOP FOR SELECTIVE ETCH OF DOPED SILICON DIOXIDE



(57) Abstract

The present invention relates to a process for selectively plasma etching a structure upon a semiconductor substrate (12) to form designated topographical structure thereon utilizing an undoped silicon dioxide layer (22) as an etch stop. In one embodiment, a substantially undoped silicon dioxide layer (22) is formed upon a layer of semiconductor material (12). A doped silicon dioxide layer (30) is then formed upon said undoped silicon dioxide layer (16). The doped silicon dioxide layer (30) is etched to create the topographical structure. The

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UNDOPED SILICON DIOXIDE AS ETCH STOP FOR SELECTIVE ETCH OF DOPED SILICON DIOXIDE

BACKGROUND OF THE INVENTION

1. The Field of the Invention

The present invention involves an etching process that utilizes an undoped silicon dioxide layer as an etch stop during a selective etch of a doped silicon dioxide layer that is situated on a semiconductor substrate. More particularly, the present invention relates to a process for selectively utilizing a fluorinated chemistry in a plasma etch system for etching a doped silicon dioxide layer situated upon an undoped silicon dioxide layer that acts as an etch stop.

2. The Relevant Technology

Modern integrated circuits are manufactured by an elaborate process in which a large number of electronic semiconductor devices are integrally formed on a semiconductor substrate. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including but not limited to bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term substrate refers to any supporting structure including but not limited to the semiconductive substrates described above.

Conventional semiconductor devices which are formed on a semiconductor substrate include capacitors, resistors, transistors, diodes, and the like. In advance manufacturing of integrated circuits, hundreds of thousands of these semiconductor devices are formed on a single semiconductor substrate. In order to compactly form the semiconductor devices, the semiconductor devices are formed on varying levels of the semiconductor substrate. This requires forming a semiconductor substrate with a topographical design.

The semiconductor industry is attempting to increase the speed at which integrated circuits operate, to increase the density of devices on the integrated circuits, and to reduce the price of the integrated circuits. To accomplish this task, the semiconductor devices used to form the integrated circuits are continually being increased in number and decreased in dimension in a process known as miniaturization.

One component of the integrated circuit that is becoming highly miniaturized is the active region. An active region is a doped area in a semiconductor substrate that is used together with other active regions to form a diode or a transistor. The miniaturization of the active region complicates the formation of the interconnect structure in that, in order to maintain sufficient electrical communication, the interconnect structure must be formed in exact alignment with the active region. Also, the area of the interconnect structure interfacing with the active region must be maximized. Thus, less area is provided as tolerance for misalignment of the interconnect structure.

The increasing demands placed upon manufacturing requirements for the interconnect structure have not been adequately met by the existing conventional technology. For example, it is difficult at greater miniaturization levels to exactly align the contact hole with the active region when patterning and etching the contact hole. As a result, topographical structures near the bottom of the contact hole upon the active region can be penetrated and damaged during etching of the contact hole. The damage reduces the performance of the active region and alters the geometry thereof, causing a loss of function of the semiconductor device being formed and possibly a defect condition in the entire integrated circuit. To remedy these problems, the prior art us s an etch stop to prevent over etching.

In a conventional self-aligned etch process for a contact hole, a silicon nitride layer or cap is usually used on top of a gate stack as an etch stop layer during the self-aligned contact etch process. One of the problems in the prior art with forming a silicon nitride cap was the simultaneous formation of a silicon nitride layer on the back side of the semiconductor wafer. The particular problems depend on the process flow. For instance, where a low pressure chemical vapor deposition is used to deposit silicon nitride, both sides of the semiconductor wafer would receive deposits of silicon nitride. The presence of the silicon nitride on the back side of the semiconductor wafer causes stress which deforms the shape of the semiconductor wafer, and can also potentially cause deformation of the crystal structure as well as cause defects in the circuit. Additionally, silicon nitride deposition is inherently a dirty operation having particulate matter in abundance which tends to reduce yield. When a low pressure chemical vapor deposition process is utilized, the silicon nitride layering on the back side of the semiconductor wafer must be removed later in the process flow.

SUMMARY OF THE INVENTION

The present invention relates to a process for selectively plasma etching a semiconductor substrate to form a designated topographical structure thereon utilizing an undoped silicon dioxide layer as an etch stop. In one embodiment, a substantially undoped silicon dioxide layer is formed upon a layer of semiconductor material. A doped silicon dioxide layer is then formed upon the undoped silicon dioxide layer. The doped silicon dioxide layer is etched to create a topographical structure. The etch has a material removal rate that is at least 10 times higher for doped silicon dioxide than for the undoped silicon dioxide or the layer of semiconductor material.

One application of the inventive process includes a multilayer structure situated on a semiconductor substrate that comprises layers of a semiconductor material, a thin silicon dioxide layer, a layer of conductor material, and a refractory metal silicide layer. By way of example, the multilayer structure situated on a semiconductor substrate may consist of a gate oxide situated on a silicon substrate, a layer of polysilicon, and a refractory metal silicide layer on the layer of polysilicon. A substantially undoped silicon dioxide layer is then formed over the multilayer structure.

The multilayer structure is then patterned to form the designated topography. Doped silicon dioxide is then formed on the semiconductor substrate as a passivation layer. A photoresist layer is utilized to expose selected portions of the doped silicon dioxide layer that are intended to be etched. One example of a topographical structure created utilizing this process are gate stacks. The doped silicon dioxide is then selectively and anisotropically etched with a carbon fluorine etch recipe so as to self-align contact holes down to the semiconductor substrate between the gate stacks.

Each gate stack has a cap composed of substantially undoped silicon dioxide. A layer of silicon nitride or undoped silicon dioxide is deposited over the gate stacks and the semiconductor substrate therebetween. A spacer etch is performed to create silicon nitride or undoped silicon dioxide spacers on the side of each gate stack. The silicon nitride or undoped silicon dioxide spacers are generally perpendicular to the base silicon layer.

The present invention contemplates a plasma etching process for anisotropic etching a doped silicon dioxide layer situated on an undoped dioxide layer that acts as an etch stop. One application of the present invention is the formation of gate stacks having spacers composed of substantially undoped silicon dioxide. The undoped silicon dioxide spacers act as an etch stop. Novel gate structures are also contemplated that use a

substantially undoped silicon dioxide etch stop layer for a carbon fluorine etch of a doped silicon dioxide layer, where the substantially undoped silicon dioxide etch stop layer resists etching by a carbon fluorine etch.

BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which the above-recited and other advantages and objects of the invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are therefore not to be considered limiting of its scope, the invention will be described with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 is a partial cross-sectional elevation view of one embodiment of a multilayer structure prior to an etch, the multi-layer structure including a base silicon layer and a layer of undoped silicon dioxide, where the multi-layer structure has a layer of photoresist, and wherein a first selected pattern is defined in phantom.

Figure 2 is a partial cross-sectional elevation view of the structure seen in Figure 1, wherein the layer of undoped silicon dioxide has been etched so as to form a recess terminating upon the base silicon layer, a layer of doped silicon dioxide has been deposited thereover, where a layer of photoresist is formed over the layer of doped silicon dioxide, and wherein a second selected pattern is defined in phantom which is intended to represent an etch through the layer of doped silicon dioxide to expose a contact on the base silicon layer that is self-aligned between the layer of undoped silicon dioxide, wherein the self-alignment of the etch is due to the selectivity of the etch to undoped silicon dioxide.

Figure 3 is a partial cross-sectional elevation view of one embodiment of a multilayer structure prior to an etch, the multilayer structure including a base silicon layer and having thereon layers of gate oxide, polysilicon, tungsten silicide, and undoped silicon dioxide, where the multi-layer structure has a layer of photoresist, and wherein a first selected pattern is defined in phantom.

Figure 4 is a partial cross-sectional elevation view of the structure seen in Figure 3, wherein gate stacks are formed upon the base silicon layer, each gate stack having a spacer on a sidewall thereof and a cap on the top thereof, the gate stacks having deposited thereover a layer of doped silicon dioxide, and a layer of photoresist is deposited upon the layer of doped silicon dioxide, wherein a second selected pattern is defined in phantom which is intended to represent a fluorinated chemical etch through the layer of doped silicon dioxide to expose a contact on the base silicon layer that is self-aligned

between the gate stacks, wherein the self-alignment of the etch is due to the selectivity of the etch to the materials of the spacers and the cap of the gate stacks.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The inventive process herein is directed towards selectively utilizing a plasma etch system on doped silicon dioxide (SiO_2) layer with a substantially undoped silicon dioxide layer as an etch stop. One application of the inventive process is to form a self-aligned contact. The present invention also discloses an inventive multilayer gate structure.

As illustrated in Figure 1, one embodiment of a multilayer structure 10 is created that comprises a base silicon layer 12. Overlying silicon base layer 12 is a substantially undoped silicon dioxide layer 22. Undoped silicon dioxide layer 22 can be any type of undoped oxide and be formed by a thermal process, by a plasma enhanced deposition process, or by a conventional TEOS precursor deposition that is preferably rich in carbon or hydrogen, or by a precursor of gaseous silane (SiH_4) with oxygen. In the latter process, the gaseous silane flow will result in undoped silicon dioxide layer 22.

The next layer in the embodiment of multilayer structure 10 illustrated in Figure 1 comprises a photoresist layer 24 that is processed to expose a first selected pattern 15, shown in phantom, such that silicon dioxide layer 22 will be used to create a topography in multilayer structure 10. Multilayer structure 10 is then anisotropically etched as shown by first selected pattern 15 to selectively remove material from undoped silicon dioxide layer 22 to form undoped silicon dioxide caps 16 as seen in Figure 2.

A doped silicon dioxide layer 30 is deposited over multilayer structure 10 as a passivation layer. Preferably, doped silicon dioxide layer 30 is substantially composed of borophosphosilicate glass (BPSG), borosilicate glass (BSG), or phosphosilicate glass (PSG). Most preferably, doped silicon dioxide layer 30 is substantially composed of silicon dioxide having doping of about 3% or more for boron and about 3% or more for phosphorus. A photoresist layer 32 is applied over doped silicon dioxide layer 30. Photoresist layer 32 is processed to expose a second selected portion 17 of doped silicon dioxide layer 30 that is intended to be etched. Second selected portion 17 is seen in phantom in Figure 2.

The structure seen in Figure 2 is now etched with a fluorinated or fluoro-carbon chemical etchant system to form second selected pattern 17 as illustrated in Figure 2. The preferred manner is an anisotropic plasma etch of doped silicon dioxide layer 30 down to the corresponding etch stop layer of undoped silicon dioxide cap 16. The plasma etch technique employed herein is preferably generated under a vacuum within the confines of a discharging unit and involves any type of a plasma system, including

a high density plasma etcher. A conventional radio frequency reactive ion etcher (RF RIE) plasma system, a magnetically enhanced RIE (MERIE) plasma system, or an inductively coupled plasma system could be used. The preferred embodiment, however, is an RF type RIE or MERIE plasma system. It is preferred the plasma system being used has a plasma density in a range from about 10^9 /cm^3 to about 10^{11} /cm^3 A high density plasma system can also be used having a plasma density in a range from about 10^{12} /cm^3 to about 10^{13} /cm^3

One particular embodiment of a specific structure created utilizing the inventive process is illustrated in Figure 3 wherein a multilayer structure 50 is created that comprises a base silicon layer 12. Overlying silicon base layer 12 is a gate oxide layer 14 that covers silicon base layer 12. Gate oxide layer 14 may be relatively thin in comparison with the other layers of the multilayered structure. The next layer in multilayer structure 50 comprises a polysilicon gate layer 18. Overlying polysilicon gate layer 18 is a refractory metal silicide layer 20. A known benefit of refractory metal silicides is their low resistivity. Refractory metal silicide layer 20 may comprise any refractory metal including but not limited to titanium, tungsten, tantalum, and molybdenum. Preferably, refractory metal silicide layer 20 is substantially composed of tungsten silicide (WSi_x).

Overlying refractory metal silicide layer 20 is a substantially undoped silicon dioxide layer 22 which can be formed thermally, by plasma enhanced deposition, by a conventional TEOS precursor deposition that is preferably rich in carbon or hydrogen, or by a precursor of gaseous silane (SiH_4) with oxygen. The next layer in multilayer structure 50 is a photoresist layer 24 that is processed to expose a first selected pattern 15 shown in phantom. Multilayer structure 50 is then etched according to first selected pattern 15 to selectively remove material so as to form gate stacks 26 as illustrated in Figure 4. Each gate stack 26 has an undoped silicon dioxide cap 52 thereon which was formed from undoped silicon dioxide layer 22.

A spacer 28 in on the sidewall of each gate stack 26. Spacers 28 are formed by subjecting a layer of silicon nitride deposited over gate stacks 26 to a spacer etch. Silicon nitride spacers 28 are generally perpendicular to silicon base layer 12. Alternatively, spacers 28 can be substantially composed of undoped silicon dioxide. As such, both spacers 28 and undoped silicon dioxide caps 52 can be made from the same materials and both act as an etch stop.

Once gate stacks 26 are formed, a contact 34 is defined therebetween upon silicon base layer 12. At this point in the processing, a doped silicon dioxide layer 30, composed of a material such as PSG, BSG, or BPSG, is deposited over multilayer structure 50. A photoresist layer 32 is then applied over doped silicon dioxide layer 30. Photoresist layer 32 is processed to create a second selected pattern 17 that is illustrated in phantom in Figure 4.

The structure seen in Figure 4 is now etched with a fluorinated or fluoro-carbon chemical etchant system according to second selected pattern 17. The preferred manner of etching of doped silicon dioxide layer 30 down to its corresponding etch stop layer, which is substantially undoped silicon dioxide layer 52, is by a plasma etch. The etch technique employed herein is preferably a plasma etch involving any type of a plasma system including a high density plasma etcher as previously discussed relative to Figure 2.

One factor that effects the etch rate and the etch selectivity of the process is pressure. The total pressure has a preferred range from about 1 millitorr to about 400 millitorr. A more preferred pressure range for a plasma etch is in a pressure range from about 1 millitorr to about 100 millitorr. The most preferred pressure range for a plasma etch is from about 1 millitorr to about 75 millitorr. The pressure may be increased, however, above the most preferred ranges. For example, the RIE etch may be performed at about 100 millitorr. Selectivity can be optimized at a pressure range between about 10 millitorr and about 75 millitorr. Pressure increases may result in a loss in selectivity. The range in selectivity, however, can be adjusted to accommodate different pressures. As such, selectivity and pressure are inversely related.

Temperature is another factor that effects the selectivity of the etching process used. A preferable temperature range during the plasma etch has a range of about 10°C to about 80°C, and more preferably about 20°C to about 40°C. This is the temperature of a bottom electrode adjacent to silicon layer 12 during the etching process. The preferable range of the semiconductor materials is between about 40°C and about 130°C, and more preferably between about 40°C and about 90°C.

Undoped silicon dioxide cap 52 and silicon nitride spacers 28 protect gate stacks 26 from the fluorinated chemical etch. As illustrated in Figure 4, the etch will selectively and anisotropically remove doped silicon dioxide layer 30 above contact 34 as indicated by second selected pattern 17. The etch removes material from doped silicon dioxide layer 30 at a higher material removal rate than that of undoped silicon dioxide

cap 52 and silicon nitride spacers or undoped silicon dioxide spacers 28. Preferably, the etch has a material removal rate for doped silicon dioxide is at least 10 times higher than that of undoped silicon dioxide. As such contact 34 is self-aligned between spacers 28 of gate stacks 26. The self-aligning aspect of contact 34 is due to the selectivity of the etch which assures that even in cases of misalignment of the exposure of second selected pattern 17, the fluorinated chemical etch through doped silicon dioxide layer 30 will properly place contact 34 on silicon base layer 12 and between adjacent silicon nitride spacers 28 that have been formed upon sides of gate stacks 26.

Contact 34 is preferably exposed by an anisotropic plasma etch with a fluorinated chemistry that etches through BSG, PSG, BPSG, or doped silicon dioxide in general. The etch is preferably selective to undoped silicon dioxide, silicon, and silicon nitride. The fluorinated chemical etch utilizes a type of carbon fluorine gas from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_2F_8, CH_2F_2, CHF_3, C_2HF_5, CH_3F and combinations thereof. There are other fluorinated enchants in a substantially gas phase during the etching of the structure. An inert gas is often used in combination with the fluorinated etchant. Argon, nitrogen, and helium are examples of such an inert gas. The preferred gasses, however, are CF_4, CH_2F_2, CHF_3 and Ar. Alternatively CH_3F may be used in place of CH_2F_2. In particular, the preferred enchant is a fluorine deficient gas which is defined as a gas where there are not enough fluorine atoms to saturate the bonding for the carbon atoms.

A conductive material is formed upon contact 34 between spacers 28 within second selected pattern 17 as shown in Figure 4. The conductive material will form a contact plug to contact 34. It may be desirable to clad the contact plug with a refractory metal or a refractory metal silicide. As such, second selected pattern 17 would have proximate thereto the refractory metal or silicide thereof prior to formation of the contact plug in contact with contact 34.

The present invention has application to a wide variety of structures. The top layer of the gate stack, composed of undoped silicon dioxide, can be used to create and protect various types of structures during the doped silicon dioxide etching process for structures other than gate stacks.

The present invention allows the gate stack height to be reduced. One advantage of reducing the gate stack height is to reduce the process time which results in greater throughput. The reduced gate height results in a lower etch time and a reduced contact hole aspect ratio, the latter being defined as the ratio of height to width of the contact

hole. By reducing the aspect ratio, or by reducing the height of the gate stack, there will be a decrease in the etch time. Another advantage of a lower gate stack height is that it reduces the overall topography which in turn results in it being easier to planarize and to use photolithographic processes. As such, the present invention increases yield.

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed and desired to be secured is:

1. A process for forming a contact opening to a semiconductor material, said process comprising:

(a) forming a substantially undoped silicon dioxide layer over a layer of semiconductor material;

(b) forming a doped silicon dioxide layer over said undoped silicon dioxide layer; and

(c) selectively removing a portion of said doped silicon dioxide layer at a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide or for said layer of semiconductor material to form an opening extending to a contact surface on said layer of semiconductor material.

2. A process as recited in Claim 1, wherein selectively removing said doped silicon dioxide layer comprises:

(a) forming a layer of photoresist over said doped silicon dioxide layer;

(b) patterning said layer of photoresist; and

(c) etching said doped silicon dioxide layer through the pattern of said layer of photoresist.

3. A process as recited in Claim 1, wherein the semiconductor material is monocrystalline silicon.

4. A process as recited in Claim 1, wherein selectively removing said doped silicon dioxide layer comprises a plasma etching process for etching said doped silicon dioxide layer in a plasma etcher.

5. A process as recited in Claim 4, wherein said plasma etching process has a plasma density in a range from about 10^9 /cm^3 to about 10^{13} /cm^3

6. A process as recited in Claim 4, wherein said plasma etching process is conducted in a pressure range from about 1 millitorr to about 400 millitorr.

7. A process as recited in Claim 4, wherein during said plasma etching process said reactor cathode has a temperature range from about 10°C to about 80°C.

8. A process as recited in Claim 4, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

9. A process as defined in Claim 1, wherein selectively removing said doped silicon dioxide layer comprises etching of said doped silicon dioxide with an etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_2F_8, CH_2F_2, CHF_3, C_2HF_5, and CH_3F.

10. A process as defined in Claim 9, wherein selectively removing said doped silicon dioxide layer comprises etching of said doped silicon dioxide with an etchant selected from the group consisting of CH_2F_2 and CH_3F.

11. A process as recited in Claim 1, wherein selectively removing said doped silicon dioxide layer comprises etching of said doped silicon dioxide with a fluorinated chemical etchant.

12. A process as recited in Claim 1, wherein said doped silicon dioxide layer is selected from the group consisting of BPSG, PSG, and BSG.

13. A process for forming contact to a semiconductor material, said process comprising:

(a) forming a substantially undoped silicon dioxide layer over a layer of monocrystalline silicon;

(b) forming a doped silicon dioxide layer over said undoped silicon dioxide layer, said doped silicon dioxide layer being selected from the group consisting of BPSG, PSG, and BSG;

(c) forming a layer of photoresist over said doped silicon dioxide layer;

(d) patterning said layer of photoresist;

(e) etching said doped silicon dioxide layer through the pattern of said layer of photoresist in a plasma etching process in a plasma etcher, said plasma etching process being conducted:

(a) at a pressure range from about 1 millitorr to about 400 millitorr;

(b) a temperature range of the cathode that is from about 10°C to about 80°C;

(c) in a plasma density in a range from about 10^9 /cm^3 to about 10^{13} /cm^3

(d) with a fluorinated chemical etchant; and

(f) whereby a contact is exposed on said layer of monocrystalline silicon.

14. A process as recited in Claim 13, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

15. A process as recited in Claim 13, wherein said fluorinated chemical etchant comprises an etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_2F_8, CH_2F_2, CHF_3, C_2HF_5, and CH_3F.

16. A process as defined in Claim 15, wherein selectively removing said doped silicon dioxide layer comprises etching of said doped silicon dioxide with an etchant selected from the group of CH_2F_2 and CH_3F.

17. A process as recited in Claim 13, wherein said plasma etching process is conducted at a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide or for said semiconductor material.

18. A process for forming a contact to a semiconductor substrate comprising:

(a) providing a gate oxide layer over the semiconductor substrate;

(b) providing a pair of gate stacks in spaced relation to one another on the semiconductor substrate, each of said gate stacks having at least one conductive layer formed therein and a substantially undoped silicon dioxide layer extending over said conductive layer;

(c) forming a spacer adjacent to each of said gate stacks;

(d) forming a doped silicon dioxide layer over said pair of gate stacks and over said exposed surface on said semiconductor substrate;

(e) selectively removing a portion of said doped silicon dioxide layer between said pair of gate stacks to expose said surface on said semiconductor substrate, while removing substantially less of said undoped silicon dioxide layer over said pair of gate stacks, wherein said etching removes doped silicon dioxide at a material removal rate that is at least 10 times higher than for each of undoped silicon dioxide, the spacer material the spacer material, and the semiconductor substrate.

19. A process as recited in Claim 18, further comprising:

(a) forming polysilicon layer over said gate oxide layer;

(b) forming a refractory metal silicide layer over said polysilicon layer; and

(c) forming a substantially undoped silicon dioxide layer over said refractory metal silicide layer.

20. A process as recited in Claim 19, further comprising selectively removing portions of said substantially undoped silicon dioxide layer, said refractory metal silicide layer, said polysilicon layer, and said gate oxide layer.

21. A process as recited in Claim 18, wherein said gate stack comprises:

(a) said substantially undoped silicon dioxide layer as the top layer thereof;

(b) a refractory metal silicide layer;

(c) a polysilicon layer; and

(d) a gate oxide layer as the bottom layer thereof.

(e)

22. A process as recited in Claim 18, wherein the spacer material is substantially composed of silicon nitride.

23. A process as recited in Claim 18, wherein the spacer material is composed of substantially undoped silicon dioxide.

24. A process as recited in Claim 18, wherein the semiconductor material is monocrystalline silicon.

25. A process as recited in Claim 18, wherein said plasma etcher is selected from the group consisting of an RF RIE etcher, a MERIE etcher, and a high density plasma etcher.

26. A process as recited in Claim 18, further comprising the step of forming a contact plug composed of a conductive material and situated between said pair of gate stacks and over said surface on said semiconductor substrate.

27. A process as recited in Claim 21, wherein said refractory metal silicide layer is tungsten silicide.

28. A process as recited in Claim 18, wherein said doped silicon dioxide layer is selected from the group consisting of BPSG, PSG, and BSG.

29. A process as recited in Claim 18, wherein selectively removing said doped silicon dioxide layer comprises:

(a) forming a layer of photoresist over said doped silicon dioxide layer;

(b) patterning said layer of photoresist; and

(c) etching said doped silicon dioxide layer through the pattern of said layer of photoresist in a plasma etching process in a plasma etcher, said plasma etching process being conducted:

(a) at a pressure range from about 1 millitorr to about 400 millitorr;

(b) a temperature range of reactor cathode that is from about 10°C to about 80°C;

(c) a temperature range of the semiconductor material is from about 40°C to about 130°C;

(d) in a plasma density in a range from about 10^9 /cm^3 to about 10^{13} /cm^3 and

(e) with a fluorinated chemical etchant.

30. A process as recited in Claim 29, wherein said fluorinated chemical etchants is selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_2F_8, CH_2F_2, CHF_3, C_2HF_5, and CH_3F.

31. A process for forming a contact to a semiconductor material comprising:

(a) depositing a gate oxide layer over a layer of silicon of a semiconductor substrate;

(b) depositing a polysilicon layer over said gate oxide layer;

(c) depositing a refractory metal silicide layer over said polysilicon layer;

(d) depositing a substantially undoped silicon dioxide layer over said refractory metal silicide layer;

(e) selectively removing portions of said substantially undoped silicon dioxide layer, said refractory metal silicide layer, said polysilicon layer, and said gate oxide layer so as to form a pair of gate stacks separated by an exposed portion of said silicon layer, each said gate stack having a lateral side substantially perpendicular to said gate oxide layer and being composed of:

(a) said substantially undoped silicon dioxide layer as the top layer thereof;

(b) said refractory metal silicide layer;

(c) said polysilicon layer; and

(d) said gate oxide layer as the bottom layer thereof;

(f) forming a spacer on the lateral side of each said gate stack from a layer of spacer material;

(g) depositing a doped silicon dioxide layer over said pair of gate stacks and over said exposed portion of said silicon layer, said doped silicon dioxide layer being is selected from the group consisting of BPSG, PSG, and BSG; and

(h) etching said doped silicon dioxide layer with a plasma etching system having a plasma density in a range from about 10^9 /cm^3 to about 10^{13} /cm^3 in an etcher selected from a group consisting of RF RIE, MERIE plasma etching system, and high density plasma etching system, said plasma etching system having a pressure range from about 1 millitorr to about 400 millitorr, said doped silicon dioxide layer being etched between said pair of gate stacks so as to expose said exposed portion of said silicon layer, said etching having a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide, said spacer material, or silicon, said etching of said doped silicon dioxide being conducted with a fluorinated chemical etchant.

32. A process as recited in Claim 31, wherein the spacer material is substantially composed of one of silicon nitride and substantially undoped silicon dioxide.

33. A process as recited in Claim 31, further comprising forming a contact plug composed of a conductive material and situated between said pair of gate stacks and over the exposed portion of said silicon layer.

34. A process as recited in Claim 34, wherein said fluorinated chemical etchant is selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_2F_8, CH_2F_2, CHF_3, C_2HF_5, and CH_3F.

35. A process as recited in Claim 31, wherein during etching of said doped silicon dioxide layer with said plasma etching system, the temperature range of said reactor cathode is from about 10°C to about 80°C.

36. A process as recited in Claim 31, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

37. A process for forming a gate structure comprising:

(a) providing a multilayer structure comprising a layer of silicon dioxide over a layer of silicon;

(b) depositing a layer of substantially undoped silicon dioxide over said multilayer structure using a precursor having a gaseous silane, hydrogen, and oxygen flow;

(c) forming a first layer of photoresist over said layer of undoped silicon dioxide;

(d) patterning said first photoresist layer to form a first pattern;

(e) etching said layer of undoped silicon dioxide and said multilayer structure through said first pattern to expose a contact surface on at least a portion of said layer of silicon;

(f) depositing a layer of a nonconductive material over said layer of undoped silicon dioxide and said contact surface on said layer of silicon;

(g) etching said layer of said nonconductive material to thereby create a spacer over a lateral side of said layer of undoped silicon dioxide and over a lateral side of said multilayer structure, said spacer being generally perpendicular to said layer of silicon;

(h) removing said first layer of photoresist;

(i) depositing a doped silicon dioxide layer over said multilayer structure;

(j) forming a said second layer of photoresist over said layer of doped silicon dioxide;

(k) patterning said second layer of photoresist to form a second pattern;

(l) etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch through said second pattern to expose said contact surface on said layer of silicon, said etching having a material removal rate that is at least 10 times greater for doped silicon dioxide than for substantially undoped silicon dioxide, photoresist, or nonconductive material;

(m) removing said second layer of photoresist; and

(n) forming a contact plug composed of a conductive material in contact with said contact surface on said layer of silicon.

38. A process as recited in Claim 37, wherein said nonconductive material is one of silicon nitride and substantially undoped silicon dioxide.

39. A process as recited in Claim 37, wherein said carbon fluorine etch is an anisotropic plasma etch using fluorinated chemical etchants selected from a group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_2F_8, CH_2F_2, CHF_3, C_2HF_5, and CH_3F.

40. A process as recited in Claim 37, wherein said multilayer structure further comprises layers of gate oxide, polysilicon, and refractory metal silicide.

41. A process as recited in Claim 37, wherein said doped silicon dioxide layer is selected from a group consisting of BPSG, PSG, and BSG.

42. A process as recited in Claim 37, wherein etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch utilizes a plasma etching system selected from a group consisting of RF RIE, MERIE system, and a high density plasma etch system.

43. A process as recited in Claim 37, wherein etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch is a plasma etching process being conducted:

(a) at a pressure range from about 1 millitorr to about 400 millitorr;

(b) a temperature range of reactor cathode that is from about 10°C to about 80°C;

(c) a temperature range of the semiconductor material is from about 40°C to about 130°C;

(d) in a plasma density in a range from about 10^9/cm3 to about 10^{13}/cm3; and

(e) with a fluorinated chemical etchant.

44. A process for forming a gate structure comprising:

(a) providing a multilayer structure situated over a layer of silicon and comprising layers of gate oxide, polysilicon, and refractory metal silicide;

(b) depositing a layer of substantially undoped silicon dioxide over said multilayer structure using a precursor having a gaseous silane, hydrogen, and oxygen flow;

(c) forming a first layer of photoresist over said layer of undoped silicon dioxide;

(d) patterning said first photoresist layer to form a first pattern;

(e) etching said layer of undoped silicon dioxide and said multilayer structure through said first pattern to expose a contact surface on at least a portion of said layer of silicon;

(f) removing said first layer of photoresist;

(g) depositing a layer of a nonconductive material over said layer of undoped silicon dioxide and said contact surface on said layer of silicon;

(h) etching said layer of said nonconductive material to thereby create a spacer over a lateral side of said layer of undoped silicon dioxide and over a lateral side of said multilayer structure, said spacer being generally perpendicular to said layer of silicon;

(i) depositing a doped silicon dioxide layer over said multilayer structure and over said contact surface on said layer of silicon, wherein said doped silicon dioxide layer is selected from a group consisting of BPSG, PSG, and BSG;

(j) forming a said second layer of photoresist over said layer of doped silicon dioxide;

(k) patterning said second layer of photoresist to form a second pattern;

(l) etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch through said second pattern to expose said contact surface on said layer of silicon, said etching having a material removal rate that is at least 10 times greater for doped silicon dioxide than for substantially undoped silicon dioxide, photoresist, or nonconductive material, wherein said carbon fluorine etch is an anisotropic plasma etch using a fluorinated chemical etchant, wherein said etching of said doped silicon dioxide

utilizes a plasma etching system having a plasma density in a range from about 10^9 /cm^3 to about 10^{13} /cm^3 at a pressure in a range from about 1 millitorr to about 400 millitorr, the temperature range of said reactor cathode during said plasma etch being about 10°C to about 80°C, and the temperature range of the semiconductor material during said plasma etch being in the range of about 40°C to about 130°C;

(m) removing said second layer of photoresist; and

(n) forming a contact plug composed of a conductive material in contact with said contact surface on said layer of silicon.

45. A process as recited in Claim 44, wherein said fluorinated chemical etchant is selected from a group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_2F_8, CH_2F_2, CHF_3, C_2HF_5, and CH_3F.

46. A process as recited in Claim 44, wherein said nonconductive material is one of silicon nitride and substantially undoped silicon dioxide.

47. A gate structure comprising:

(a) a pair of gate stacks situated over a base silicon layer, each said gate stack comprising:

(a) a gate oxide layer on said base silicon layer;

(b) a polysilicon gate layer on said gate oxide layer;

(c) a layer of refractory metal silicide on said polysilicon gate layer;

(d) a substantially undoped silicon dioxide cap on said layer of refractory metal silicide;

(b) a spacer in contact with a lateral side of each said gate stack and with said base silicon layer, said spacer being composed of a nonconductive material, each said lateral side of each said gate stack being substantially perpendicular to said base silicon layer;

(c) a contact plug in contact with said base silicon layer composed of a conductive material, and being situated between said pair of gate stacks; and

(d) a layer of doped silicon dioxide over said spacer, over said substantially undoped silicon dioxide cap, and in contact with said contact plug.

48. A gate structure as recited in Claim 47, wherein said nonconductive material is substantially composed of silicon nitride.

49. The gate structure as recited in Claim 47, wherein said nonconductive material is substantially composed of substantially undoped silicon dioxide, and each said spacer is integral with a respective one of said substantially undoped silicon dioxide cap.

50. A method of forming a self-aligned contact, said method comprising:

(a) providing a pair of gate stacks in spaced apart relation to one another on said semiconductor substrate, each of said gate stacks being covered by a substantially undoped silicon dioxide layer;

(b) forming a spacer adjacent to each of said gate stacks;

(c) forming a doped silicon dioxide layer over said pair of gate stacks and over said semiconductor substrate;

(d) forming a layer of photoresist over said silicon dioxide layer;

(e) patterning said layer of photoresist; and

(f) selectively removing a portion of said doped silicon dioxide layer between said pair of gate stacks to expose a contact surface on said semiconductor substrate through said pattern of said layer of photoresist, while removing substantially less of said undoped silicon dioxide layer over said pair of gate stacks than doped silicon photoresist, , said undoped silicon layer being capable of resisting said selective removal process thereby causing said selective removal process to be self-aligning between said pair of gate stacks.

51. A method as recited in Claim 50, wherein said selective removal of said doped silicon dioxide layer comprises etching said doped silicon dioxide layer in a plasma etching process being conducted:

(a) at a pressure range from about 1 millitorr to about 400 millitorr;

(b) a temperature range of the cathode that is from about 10°C to about 80°C;

(c) in a plasma density in a range from about 10^9 /cm^3 to about 10^{13} /cm^3 and

(d) with a fluorinated chemical etchants.

52. A method as recited in Claim 51, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

53. A method as recited in Claim 51, wherein said fluorinated chemical etchant comprises an etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_2F_8, CH_2F_2, CHF_3, C_2HF_5, and CH_3F.

54. A method as recited in Claim 50, wherein said plasma etching process is conducted at a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide or for semiconductor material.

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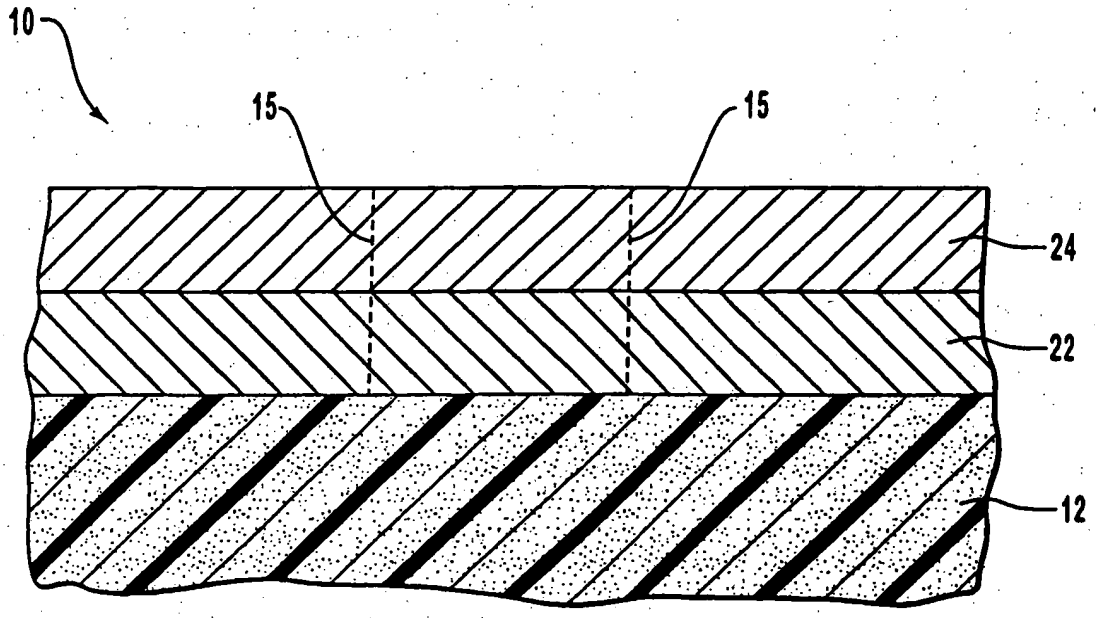

FIG. 1

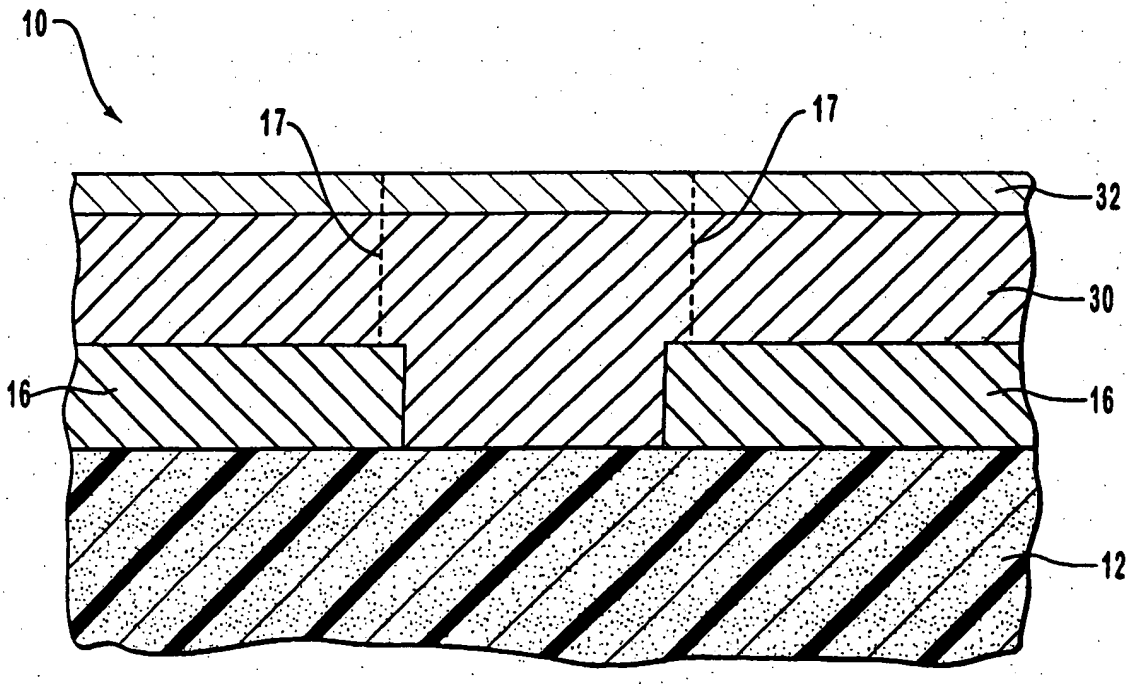

FIG. 2

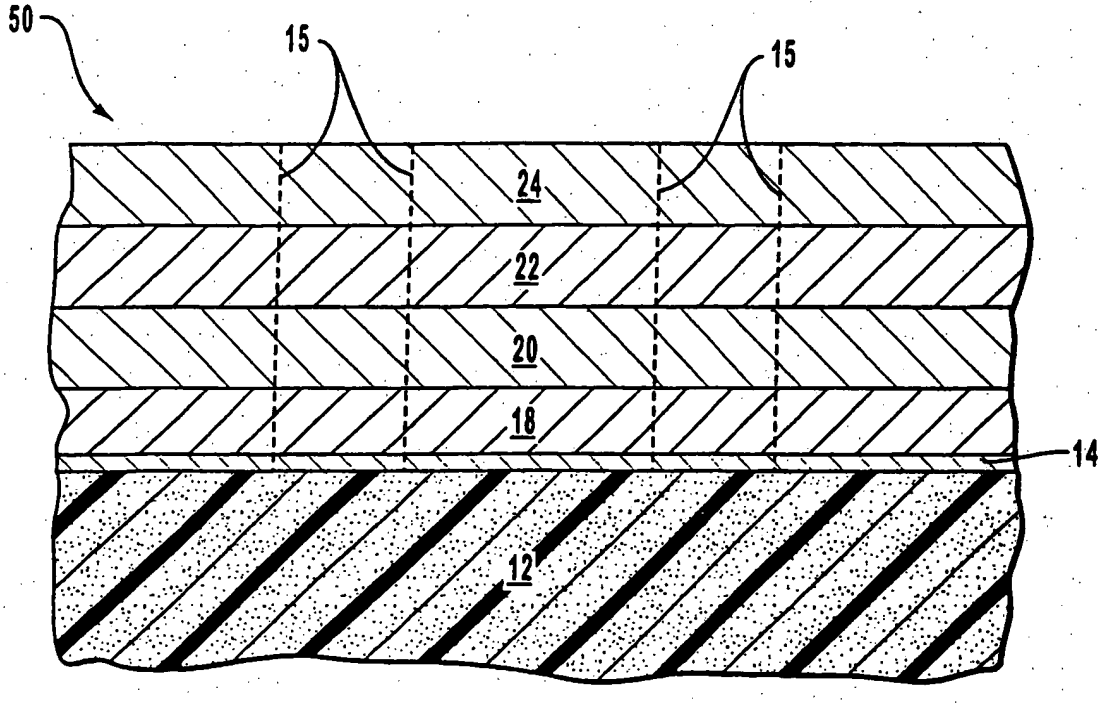
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FIG. 3

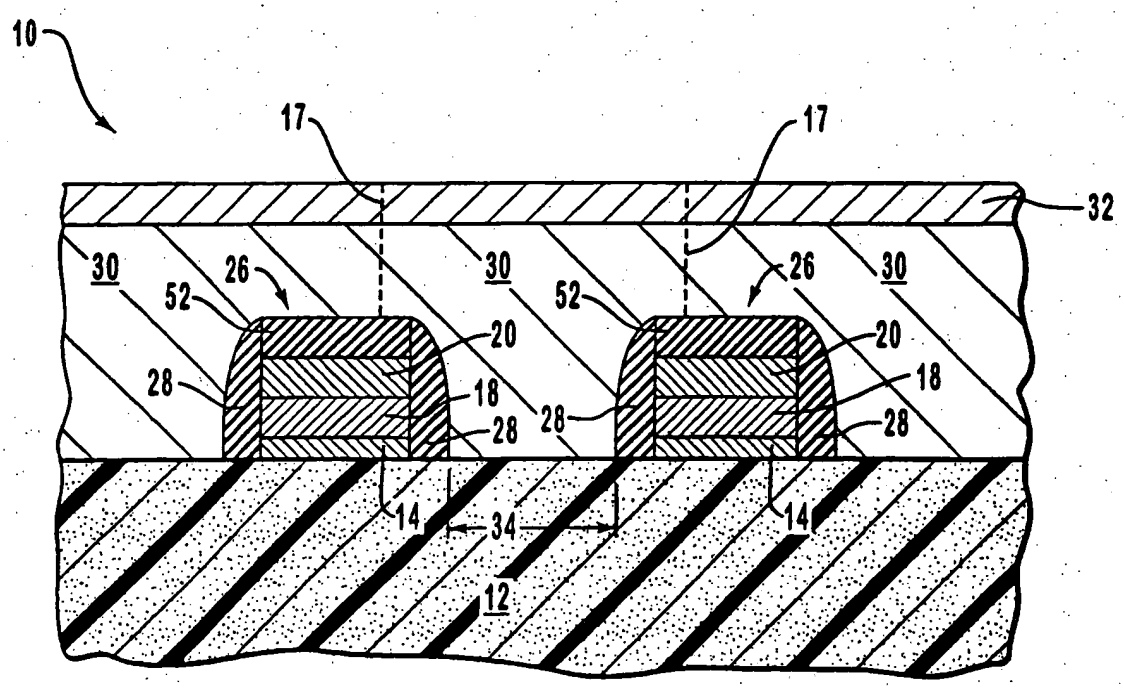
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FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/02826

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/302
US CL : 438/696,697,723,724,738,740,742,743,744

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/696,697,723,724,738,740,742,743,744

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS:USPAT; STN: CAS; Orbit: WPAT, JAPIO, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,286,344 A (BLALOCK ET AL) 15 February 1994 (15-02-94), columns 5-9, Figs. 1-2.	1-54
A	US 5,366,590 A (KADOMURA) 22 November 1994 (22-11-94), columns 4-7, Figs. 2a-2b.	1-54
A	US 5,423,945 A (MARKS ET AL) 13 June 1995 (13-06-95), columns 1-4.	1-54
Y,P	US 5,677,227 A (YANG ET AL) 14 October 1997 (14-10-97), columns 3-7, Figs. 3-6.	1-9, 11-15, 17
A,P		10, 16, 18-54

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 MAY 1998	16 JUN 1998
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks	Authorized officer

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/02826

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US 5,626,716 A (BOSCH ET AL) 06 May 1997 (06-05-97), columns 5-8, Fig. 1.	1-9, 11
A,P		10, 12-54

SILICON PROCESSING FOR THE VLSI ERA

VOLUME 1:

PROCESS TECHNOLOGY

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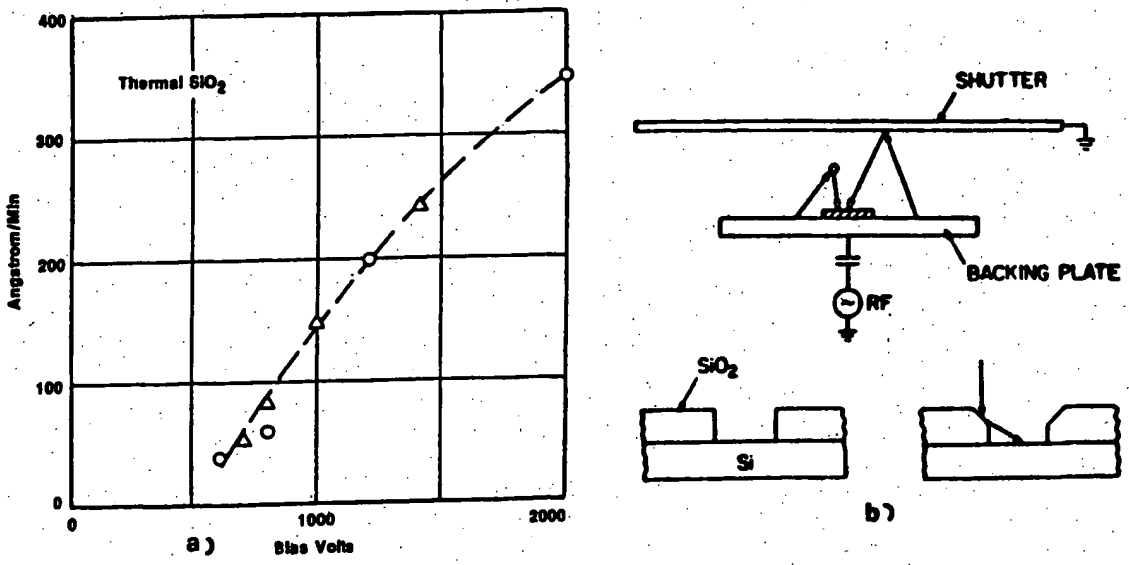


Fig. 4 (a) Example of sputter-etch rate of thermal SiO_2. Courtesy of Varian Associates. Contamination of contacts during sputter etching by (b) backscattering events, and (c) faceting. Material sputtered from the facet deposits in the contact at a rate that can exceed removal of material from the bottom of the opening[10]. Reprinted by permission of the American Physical Soc.

(2000-3000 lb /in^2) DI water jet sweeps across the wafer surface and removes the microscopic debris dislodged by the brush, as well as any residual particles generated by the brush.

In-Situ Sputter Etch Removal of Native Oxide Films

A thin oxide (5-50 Å) grows on silicon (SiO_2) or aluminum (Al_2O_3) when these materials are exposed to air. This thin oxide (known as *native oxide*) can adversely effect subsequent processing steps, for example by causing high contact resistance, or impeding interfacial reactions of films deposited on the substrate materials. Thus, it is important to remove this oxide layer and keep it from reforming before depositing the overlying film.

Concerns have arisen about whether chemical cleaning techniques will be adequate for removing native oxide films, especially in contact holes or via regions smaller than 2 μm. As a result removal of such films is also being conducted in the same vacuum environment in which the overlying film will be deposited (*in situ*). Sputter etching is used to remove up to several hundred angstroms of the wafer surface including, it is surmised, the unwanted native oxide at the bottom of the contacts or vias. Some questions have also been raised about the effectiveness of this technique for small (e.g. < 2 μm) contacts[10]. It is argued that such sputter etching (Fig. 4) will cause more contamination of the contacts through redeposition by backscattering of material sputtered from wafers and chamber surfaces, and by sputtering of contact sidewall material into the contact bottom. *In situ* removal of the native oxide by plasma chemical reactions, instead of physical sputtering mechanisms, has been proposed to circumvent this problem. Several sputter equipment suppliers offer such alternative *in situ* cleaning capabilities.

TERMINOLOGY OF ETCHING

Etching in microelectronic fabrication is a process by which material is removed from the silicon substrate or from thin films on the substrate surface. When a *mask layer* is used to protect specific regions of the wafer surface, the goal of etching is to precisely remove the

material which is not covered by the mask (Fig. 5). In this section we will discuss the terms used to describe the basic aspects of etch processes.

Bias, Tolerance, Etch Rate, and Anisotropy

In general an ideal etch process is not completely attainable. That is, the etching processes are not capable of precisely transferring the pattern established by the protective mask into the underlying material. The degree to which the process fails to satisfy the ideal is specified by two parameters: *bias* and *tolerance*. As shown in Fig. 6d, *bias* is the difference in lateral dimension between the etched image and the mask image. *Tolerance* is a measure of the statistical distribution of bias values that characterizes the uniformity of etching. The tolerance parameter can be specified for a single wafer (bias distribution across a wafer), for an entire lot (bias distribution throughout the lot) or from run-to-run (bias distribution across a group of runs).

The rate at which material is removed from the film by etching is known as the *etch rate*. The units of etch rate are typically expressed in Å /sec, μm /min, etc. Generally, high etch rates are desirable as they allow higher production throughputs, but in some cases high etch rates make control of lateral etching a problem. That is, since material removal can occur in both the horizontal and vertical directions, the *horizontal etch rate* as well as the *vertical etch rate* may need to be established in order to characterize an etch process. Normally the uniformity of these etch rates is also of interest, and is expressed for three conditions (across a wafer, from wafer-to-wafer, and from run-to-run), as *etch rate % uniformity*, according to:

$$\text{Etch Rate Percent Uniformity} = \frac{(\text{Etch Rate}_{high} - \text{Etch Rate}_{low})}{(\text{Etch Rate}_{high} + \text{Etch Rate}_{low})} \times 100\% \qquad (1)$$

Highly uniform etch rates are almost always desirable in an etch process.

The lateral etch ratio, L_R, is defined as the ratio of the etch rate in a horizontal direction to

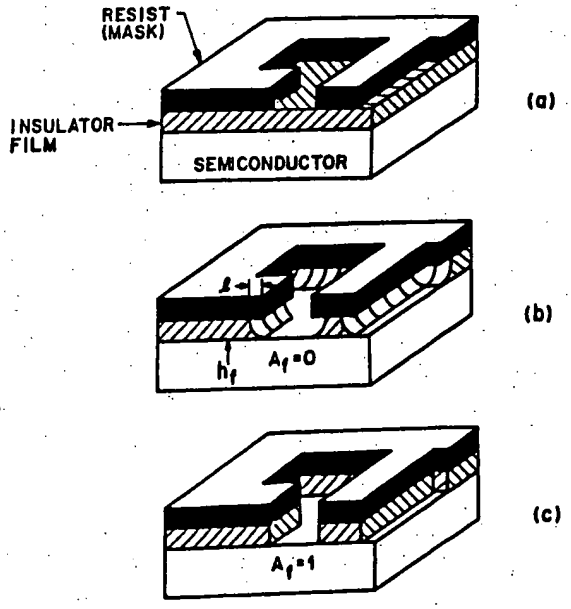


Fig. 5 Comparison of (b) isotropic, and (c) completely anisotropic etching. From E.C. Douglas, *Solid State Tehnol.*, 24, 65, (1981). Reprinted with permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet.

that in the vertical direction. Thus:

$$L_R = \frac{\text{Horizontal Etch Rate of Material}}{\text{Vertical Etch Rate of Material}} \quad (2)$$

In the case of an ideal etch process the mask pattern would be transferred to the underlying layer with zero bias. This would then create a vertical edge profile in the etched layer coincident with original edge of the mask. Therefore the lateral etch rate would also have to have been zero. For non-zero L_R, the film material is etched to some degree under the mask and this effect is called *undercut* (Fig. 5d).

When the etching can proceed in all directions at the same rate, it is said to be *isotropic* (Fig. 5b). By definition, however, any etching that is not isotropic is *anisotropic*. If etching proceeds exclusively in one direction (e.g. only vertically), the etching process is said to be *completely anisotropic*. Since many etch processes fall between the extremes of being isotropic and completely anisotropic, it is useful to define a degree of anisotropy, A, as:

$$A = 1 - L_R \quad (3)$$

Thus, when $L_R = 0$, $A = 1$, and this condition corresponds to completely anisotropic etching. When $L_R = 1$, the vertical and horizontal etch rates are equal, and the degree of anisotropy is $A = 0$. This corresponds to an isotropic etching condition. Most wet etching processes and some dry-etching processes exhibit uniform etch rates in all directions, and hence are isotropic.

An example of an etch profile in the film being removed versus time is shown for an isotropic etch, $L_R = 1$ (Fig. 6a) and for a process in which $L_R = 0.1$ (Fig. 6b). If the films are etched just to completion, the profile for $L_R = 1$ has the shape of a quarter circle, whereas the profile of $L_R = 0.1$ is vertical except near the bottom (where it is rounded). If this etch is allowed to continue, however, even the profile with $L_R = 1$ becomes more vertical, though

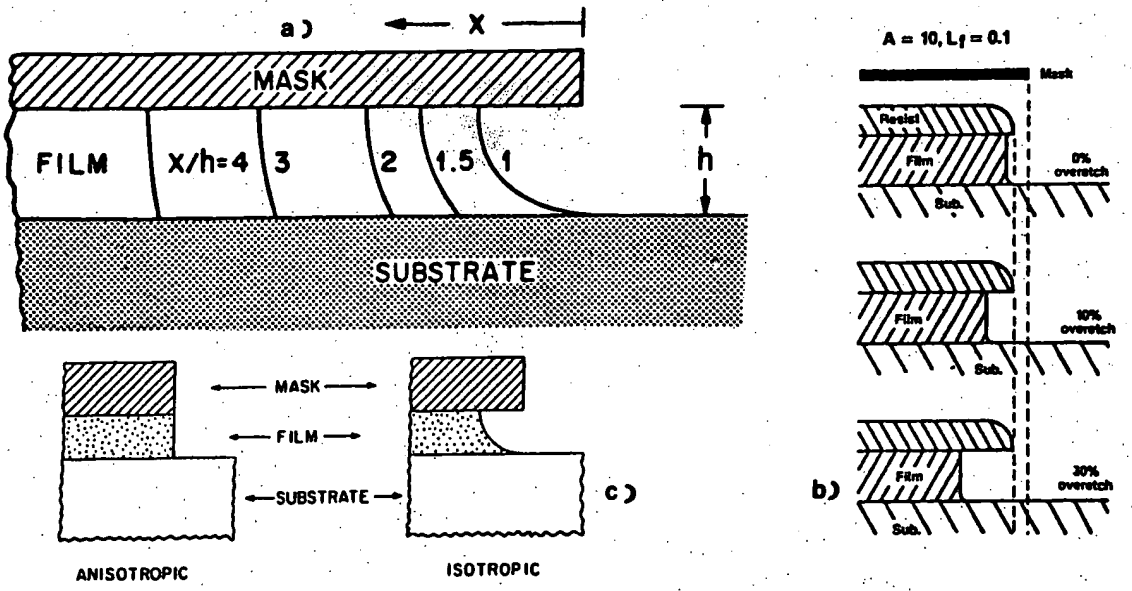


Fig. 6 (a) Isotropic etching of a film vs time ($L_R = 1$). Overetching results in pr files are more vertical. (b) Etching of film versus time when $L_R = 0.1$. (c) Etch bias is a measure of the amount by which the etched film undercuts the mask at the mask film interface. Fig. (c) Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted by permission.

lateral etching proceeds more rapidly than the process in which $L_R = 0.1$, and thus leads to more severe undercutting. As a result, we see that L_R is one of the variables which impacts feature size, as well as edge profile. We shall also see that other parameters play a role in controlling such characteristics of the feature attributes as size and edge profile.

In fabrication technologies that are performed using isotropic etching processes, the problem of etch bias is handled by specifying an appropriate amount of compensation in the mask dimensions. For example, if the bias of an etch process is 1 μm, a 6 μm feature on the *mask* can be used to produce a desired 5 μm feature on the *wafer*. Unfortunately, for VLSI technologies in which the pattern dimensions approach the thicknesses of the films being patterned, the margin for compensation diminishes, and a higher degree of anisotropy is required. For practical purposes this situation arises when pattern features become smaller than ~3 μm. Under these circumstances, isotropic etching processes become inadequate, and processes that provide higher degrees of anisotropy need to be employed.

Selectivity, Over-Etch, and Feature Size Control

In earlier sections, only the etching characteristics of the film were considered when examining the relationship between bias and edge profile, and degree of etch anisotropy. We assumed that the mask was not attacked by the etchant, and did not consider that the layers under the etched film can also be attacked by the etchant. In fact, both mask material and underlying layer materials are generally etchable, and these effects may play a significant role in specifying etch processes. Note that the underlying material subject to etchant attack may be either the silicon wafer itself, or a film grown or deposited during a previous fabrication step. The ratio of etch rates of different materials is known as the *selectivity of an etched process*[12]. Thus both: 1) the selectivity with respect to the mask material; and 2) the selectivity with respect to the substrate materials are important characteristics of an etch process.

The *selectivity with respect to the mask material*, S_{fm}, plays a role in determining the etched feature sizes. The *selectivity with respect to substrate*, S_{fs}, can impact performance and yield. Film thickness and etch rate non-uniformities increase the required values of S_{fm} and S_{fs} because the etch processes need to be continued beyond the point at which the mean film thickness is completely etched (cleared). Such additional etching is referred to as *overetch*. For example, due to overetch requirements, when contact holes are to be etched in SiO_2 it is desirable that the etch rate decrease when the silicon substrate is reached. In this case, a process with high selectivity with respect to substrate is necessary.

For many wet-etch processes, both S_{fm} and S_{fs} are very high, and thus neither the mask or substrate materials are affected very much during such well-controlled wet-etch procedures. However for dry-etch processes, these desirable circumstances are rarely encountered. Thus, it is necessary to calculate the selectivities that an etching application will require, so that dry-etch processes which are able to meet such specifications can be selected or developed.

Determining the Required Selectivity With Respect to Mask Materials, S_{fm}

The required selectivity with respect to the mask, S_{fm} is dependent on several factors including: a) film thickness uniformity; b) film etch rate uniformity; c) mask etch rate uniformity; d) the edge profile of the mask; e) the anisotropic etch rate of the mask; and f) the maximum acceptable loss of line width of the patterns being etched[11]. These factors can be quantified with the assistance of the information given in Fig. 7.

Etch Rates for Micromachining and IC Processing

U.C. Berkeley Microfabrication Laboratory
Berkeley Sensor & Actuator Center
Kirt R. Williams

The top etch rate was measured by the author with fresh solutions,
clean chambers, etc.
The center and bottom values are the low and high etch rates observed
by the author and others using fresh and used solutions,
clean and "dirty" chambers, etc.

See the accompanying paper for descriptions of etch preparation and
material, suitable masks, and etch-rate variation.

Notation:
=test not performed;
W=not performed, but known to Work (>= 100 A/min);
F=not performed, but known to be Fast (>= 10 kA/min);
P=some of film \fIP\fReeled during etch or when rinsed;
A=film was visibly \fIA\fRttacked and roughened.

Rates measured are rounded to two significant figures.

Etch areas are all of a 4-inch wafer for the transparent films
and half of the wafer for single-crystal silicon and the metals.

Etch rates will vary with temperature and prior use of solution
or plasma chamber, area of exposure of film,
other materials present (e.g., photoresist),
film impurities and microstructure, etc.
Some variation should be expected!

ETCHANT EQUIPMENT CONDITIONS	TARGET MATERIAL	MATERIAL UNDER ETCH													
SCSi+Poly+Poly+Wet 100 +npls+undp+Ox	+Dry +Ox	+LTO +undp+unan+anld+Nitd+Nitd+2%Si+Tung+Ti	+PSG	+PSG	+Stoc+LoSt+Al/		+Sput+Sput+Sput+OCG +Oln +Ti/W+820P+PR								
Concentrated HF (49%)+ Wet Sink+ Room Temperature+	Silicon oxides														
+0	+-	+23k +F	+>14k+F	+36k	+140	+52	+42	+<50 +F	+-	+P	0+P	0			

```
    +    +    +18k +    +    +    +    +    +30  +0
    +    +    +23k +    +    +    +    +    +52  +42
=============================================================================
10:1 HF+                                          Silicon
Sink 6+                                           oxides
Room Temperature     +
-----------------------------------------------------------------------------
    +7   +0   +230 +230 +340 +15k +4700+11  +3   +2500+0   +11k +<70 +0   +0
    +    +    +    +    +    +    +    +    +    +2500
    +    +    +    +    +    +    +    +    +    +12k
=============================================================================
25:1 HF+                                          Silicon
Sink 6+                                           oxides
Room Temperature+
-----------------------------------------------------------------------------
    +0   +0   +97  +95  +150 +-   +1500+6   +1   +W   +0   +-   +-   +0   +0
=============================================================================

====+====+====+====+====+====+====+====+====+====+====+====+====+====+====+====
SCSi+Poly+Poly+Wet +Dry +LTO +PSG +PSG +Stoc+LoSt+Al/ +Sput+Sput+Sput+OCG +Oln
100 +npls+undp+Ox  +Ox  +undp+unan+anld+Nitd+Nitd+2%Si+Tung+Ti  +Ti/W+820P+PR
====+====+====+====+====+====+====+====+====+====+====+====+====+====+====+====

=============================================================================
5:1 BHF+                                          Silicon
Sink 8+                                           oxides
Room Temperature+
-----------------------------------------------------------------------------
    +9   +2   +1000+1000+1200+6800+4400+9   +4   +1400+<20 +F   +1000+0   +0
    +    +    +900 +    +    +    +3500+    +3   +    +0.25
    +    +    +1080+    +    +    +4400+    +4   +    +20
=============================================================================
Phosphoric Acid (85%)+                            Silicon
Sink 7 Heated Bath+                               nitrides
160C
-----------------------------------------------------------------------------
    +7   +-   +0.7 +0.8 +<1  +37  +24  +28  +19  +9800+-   +-   +-   +550 +390
    +    +    +    +    +    +    +9   +28  +19
    +    +    +    +    +    +    +24  +42  +42
=============================================================================
Silicon Etchant (50 HNO3:20 H2O:1 NH4F)+          Silicon
Sink 8+
Room Temperature+
-----------------------------------------------------------------------------
1500+3100+1000+87  +W   +110 +4000+1700+2   +3   +4000+130 +3000+-   +0   +0
    +1200
    +6000
=============================================================================

====+====+====+====+====+====+====+====+====+====+====+====+====+====+====+====
SCSi+Poly+Poly+Wet +Dry +LTO +PSG +PSG +Stoc+LoSt+Al/ +Sput+Sput+Sput+OCG +Oln
100 +npls+undp+Ox  +Ox  +undp+unan+anld+Nitd+Nitd+2%Si+Tung+Ti  +Ti/W+820P+PR
====+====+====+====+====+====+====+====+====+====+====+====+====+====+====+====

=============================================================================
KOH (1 KOH:2 H2O by weight)+                      <100> Si
Sink 3 Heated Bath+
80C
-----------------------------------------------------------------------------
14k +>10k+F   +77  +-   +94  +W   +380 +0   +0   +F   +0   +-   +-   +F   +F
    +    +    +41
    +    +    +77
=============================================================================
Aluminum Etchant Type A+                          Alumnium
```

Sink 8 Heated Bath+
50C+

+<10 +<9	+0	+0	+0	+-	+<10 +0		+2	+6600+-		+0	+-	+0	+0	
+ +	+	+	+	+	+	+	+	+2600						
+ +	+	+	+	+	+	+	+	+6600						

SCSi+Poly+Poly+Wet	+Dry	+LTO	+PSG	+PSG	+Stoc+LoSt+Al/		+Sput+Sput+Sput+OCG									+Oln
100 +npls+undp+Ox	+Ox	+undp+unan+anld+Nitd+Nitd+2%Si+Tung+Ti					+Ti/W+820P+PR									

Titanium Etchant (20 H2O:1 H2O2:1 HF)+ Titanium
Wet Sink+
Room Temperature+

+12	+-	+120	+W	+W	+W	+2100+8		+4	+W	+0	+8800+-		+0	+0
+	+	+	+	+	+	+	+	+	+	+0				
+	+	+	+	+	+	+	+	+	+	+<10				

H2O2 (30%)+ Tungsten
Wet Sink+
Room Temperature+

+0	+0	+0	+0	+0	+0	+0	+0	+0	+<20	+190	+0	+60	+<2	+0	
+	+	+	+	+	+	+	+	+	+	+190	+	+60			
+	+	+	+	+	+	+	+	+	+	+1000	+	+150			

Piranha (~50 H2SO4:1 H2O2)+ Clean off
Sink 8 Heated Bath+ metals and
120C+ organics

+0	+0	+0	+0	+0	+-	+0	+0	+0	+1800+-		+2400+-		+F	+F

SCSi+Poly+Poly+Wet	+Dry	+LTO	+PSG	+PSG	+Stoc+LoSt+Al/		+Sput+Sput+Sput+OCG									+Oln
100 +npls+undp+Ox	+Ox	+undp+unan+anld+Nitd+Nitd+2%Si+Tung+Ti					+Ti/W+820P+PR									

Acetone+ Photoresist
Sink 5+
Room Temperature+

+0	+0	+0	+0	+0	+-	+0	+0	+0	+0	+-	+0	+-	+>44k+>39k	

HF Vapor+ Silicon
Wet sink--1 cm over plastic dish+ oxides +
Room temperature and pressure+

+0	+0	+660	+W	+780	+2100	+1500	+10	+19	+A	+0	+A	+-	+P	0+P	0

XeF2$+ Silicon
Old lab--Simple custom vacuum chamber
Room temperature, 2.6 Torr

4600+1900+1800+0	+-	+0	+0	+0	+120	+2	+0	+800	+290	+-	+0	+0			
+2900+1100+1100+	+	+	+	+	+120	+0	+	+440	+50						
+100k+2500+2300+	+	+	+	+	+180	+2	+	+1000	+380						

```
====+====+====+====+====+====+====+====+====+====+====+====+====+====+====+====
SCSi+Poly+Poly+Wet +Dry +LTO +PSG +PSG +Stoc+LoSt+Al/ +Sput+Sput+Sput+OCG +Oln
100 +npls+undp+Ox  +Ox  +undp+unan+anld+Nitd+Nitd+2%Si+Tung+Ti  +Ti/W+820P+PR
====+====+====+====+====+====+====+====+====+====+====+====+====+====+====+====

==========================================================================
SF6+He (175:50 sccm)--In THINSTD.RCP+          Thin
Lam 1--Lam 480 Plasma+                        silicon
150W, 375mT, gap=1.35cm, 13.56MHz+            nitrides
--------------------------------------------------------------------------
W   +6400+7000+300 +W   +280 +530 +540 +1300+870 +-   +W   +W   +W   +1500+1400
    +    +2000+220 +    +    +    +    +830 +    +    +    +    +    +1300+
    +    +7000+400 +    +    +    +    +2300+    +    +    +    +    +1500+
==========================================================================
SF6+He (175:50 sccm)--In NITSTD1.RCP+          Thick
Lam 1--Lam 480 Plasma+                        silicon
250W, 375mT, gap=1.35cm, 13.56MHz+            nitrides
--------------------------------------------------------------------------
W   +8400+9200+800 +W   +770 +1500+1200+2800+2100+-   +W   +W   +W   +3400+3100
    +    +    +    +    +    +    +    +2100+    +    +    +    +    +3100+
    +    +    +    +    +    +    +    +4200+    +    +    +    +    +3400+
==========================================================================
CF4+CHF3+He (90:30:120 sccm)+                 Silicon
Lam 2--Lam 590 Plasma+                        oxides
450W, 2.8T, gap=0.38cm, 13.56MHz+
--------------------------------------------------------------------------
W   +1900+2100+4700+W   +4500+7300+6200+1800+1900+-   +W   +W   +W   +2200+2000
    +1400+1500+2400+    +    +3000+2500
    +1900+2100+4800+    +    +7300+7200
==========================================================================

====+====+====+====+====+====+====+====+====+====+====+====+====+====+====+====
SCSi+Poly+Poly+Wet +Dry +LTO +PSG +PSG +Stoc+LoSt+Al/ +Sput+Sput+Sput+OCG +Oln
100 +npls+undp+Ox  +Ox  +undp+unan+anld+Nitd+Nitd+2%Si+Tung+Ti  +Ti/W+820P+PR
====+====+====+====+====+====+====+====+====+====+====+====+====+====+====+====

==========================================================================
CF4+CHF3+He (90:30:120 sccm)--In SIO2ET.RCP+  Silicon
Lam 2--Lam 590 Plasma+                        oxides
850W, 2.8T, gap=0.38cm, 13.56MHz+
--------------------------------------------------------------------------
W   +2200+1700+6000+W   +6400+7400+6700+4200+3800+-   +W   +W   +W   +2600+2900
    +2200+1700+2500+    +6000+5500+5000+4000+    +    +    +    +    +2600+2900
    +2700+2100+7600+    +6400+7400+6700+6800+    +    +    +    +    +6700+7200
==========================================================================
Cl2+BCl3+CHCl3+N sub 2 (30:50:20:50 sccm)+    Aluminum
Lam 3--Lam 690 RIE+
250W, 250mT, 60\(deC, 13.56MHz+
--------------------------------------------------------------------------
W   +4500+W   +680 +670 +750 +W   +740 +930 +860 +6000+W   +-   +-   +6300+6300
    +    +    +    +    +    +    +    +    +    +1900+    +    +    +3700+3300
    +    +    +    +    +    +    +    +    +    +6400+    +    +    +6300+6100
==========================================================================
Cl2+He (180:400 sccm)--In Rec. 400,500,550+   Silicon
Lam 4--Lam Rainbow 4420 Plasma+
275W, 425mT, 40\(deC, gap=0.80cm, 13.56MHz+
--------------------------------------------------------------------------
W   +5700+3200+8   +-   +60  +230 +140 +560 +530 +W   +W   +-   +-   +3000+2700
5000+3400+3200+8   +    +    +    +    +    +    +    +    +    +    +2400
5000+6300+3700+380 +    +    +    +    +    +    +    +    +    +    +3000
==========================================================================

====+====+====+====+====+====+====+====+====+====+====+====+====+====+====+====
SCSi+Poly+Poly+Wet +Dry +LTO +PSG +PSG +Stoc+LoSt+Al/ +Sput+Sput+Sput+OCG +Oln
```

```
100 +npls+undp+Ox  +Ox  +undp+unan+anld+Nitd+Nitd+2%Si+Tung+Ti  +Ti/W+820P+PR
====+====+====+====+====+====+====+====+====+====+====+====+====+====+====+====

==========================================================================
HBr+Cl2 (70:70 sccm)--In Rec. 500,550+          Silicon
Lam 4--Lam Rainbow 4420 Plasma+
200W, 300mT, 40\(deC, gap=0.80cm, 13.56MHz+
--------------------------------------------------------------------------
W   +450 +460 +4   +-   +0   +0   +0   +870 +26  +W   +W   +-   +-   +350 +300
    +450 +    +4   +    +    +    +    +    +    +    +    +    +    +350
    +7400+    +100 +    +    +    +    +    +    +    +    +    +    +500
==========================================================================
O2 (51 sccm)+                                   Descumming
Technics-c--Technics PE II-A Plasma+            photoresist
50W, 300mT, gap\(~=2.6cm, 50kHz sq. wave+
--------------------------------------------------------------------------
   +0   +0   +0   +0   +0   +0   +0   +0   +0   +0   +0   +0   +-   +350 +300
==========================================================================
O2 (51 sccm)+                                   Ashing
Technics-c--Technics PE II-A Plasma+            Photoresist
400W, 300mT, gap\(~=2.6cm, 50kHz sq. wave+
--------------------------------------------------------------------------
   +0   +0   +0   +0   +0   +0   +0   +0   +0   +0   +0   +0   +-   +3400+3600
==========================================================================

====+====+====+====+====+====+====+====+====+====+====+====+====+====+====+====
SCSi+Poly+Poly+Wet +Dry +LTO +PSG +PSG +Stoc+LoSt+Al/ +Sput+Sput+Sput+OCG +Oln
100 +npls+undp+Ox  +Ox  +undp+unan+anld+Nitd+Nitd+2%Si+Tung+Ti  +Ti/W+820P+PR
====+====+====+====+====+====+====+====+====+====+====+====+====+====+====+====

==========================================================================
SF6+He (13:21 sccm)+                            Silicon
Technics-c--Technics PE II-A Plasma+            nitrides
100W, 250mT, gap\(~=2.6cm, 50kHz sq. wave+
--------------------------------------------------------------------------
300 +730 +670 +310 +350 +370 +610 +480 +820 +620 +-   +W   +W   +W   +690 +630
300 +730 +670 +    +    +    +    +230 +    +550 +    +    +    +    +690
1000+800 +760 +    +    +    +    +480 +    +800 +    +    +    +    +830
==========================================================================
CF4+CHF3+He (10:5:10 sccm)+                          Silicon
Technics-c--Technics PE II-A Plasma+            nitrides
200W, 250mT, gap\(~=2.6cm, 50kHz sq. wave+
--------------------------------------------------------------------------
1100+1900+W   +730 +710 +730 +W   +900 +1300+1100+-   +W   +W   +W   +690 +600
==========================================================================
SF6 (80 sccm)+                                  Tungsten
Tegal--Tegal Inline Plasma 701+
200W, 150mT, 40\(deC, 13.56MHz+
--------------------------------------------------------------------------
W   +5800+5400+1200+W   +1200+1800+1500+2600+2300+-   +2800+W   +W   +2400+2400
    +    +    +2000+    +    +    +    +    +1900+    +2800+    +    +2400
    +    +    +2000+    +    +    +    +    +2300+    +4000+    +    +4000
==========================================================================

====+====+====+====+====+====+====+====+====+====+====+====+====+====+====+====
SCSi+Poly+Poly+Wet +Dry +LTO +PSG +PSG +Stoc+LoSt+Al/ +Sput+Sput+Sput+OCG +Oln
100 +npls+undp+Ox  +Ox  +undp+unan+anld+Nitd+Nitd+2%Si+Tung+Ti  +Ti/W+820P+PR
====+====+====+====+====+====+====+====+====+====+====+====+====+====+====+====

==========================================================================
SF6 (25 sccm)+                                  Thin
Tegal--Tegal Inline Plasma 701+                 silicon
125W, 200mT, 40\(deC   +                        nitrides
--------------------------------------------------------------------------
```

```
W   +1700+2800+1100+W   +1100+1400+1400+2800+2300+-   +W   +W   +W   +3400+3100
    +    +    +1100+    +    +    +    +2800+    +    +    +    +    +2900
    +    +    +1600+    +    +    +    +2800+    +    +    +    +    +3400
=============================================================================
CF4+CHF3+He (45:15:60 sccm)+                  Si-rich
Tegal--Tegal Inline Plasma 701+               silicon     +
100W, 300mT, 13.56MHz+                        nitrides    +
-----------------------------------------------------------------------------
W   +350 +360 +320 +W   +320 +530 +450 +760 +600 +-   +W   +W   +W   +400 +360
=============================================================================
```

P. Riehl

Chapter 1.5

VLSI Etchants

Notes on Etch Rate Tests

For complete text, see "Etch Rates for Micromachining Processing" by Kirt R. Williams and Richard S. Muller, IEEE Journal of Microelectromechanical Systems, Vol. 5, No. 4, December 1996.

Sample preparation and etchants are discussed on the following pages. Measurement techniques and other notes are given below.

Transparent Films (poly, oxides, nitrides, photoresists) were coated over the entire wafer and etched unpatterned. Their thicknesses were measured on the Nanospec using refractive indices determined by ellipsometry and verified with the Nanospec. These RIs are listed in the samples section of this report. (The RI of my low-stress nitride films was significantly different using the Nanospec than the ellipsomet r. I used the ellipsometer RI, which agreed with published data.)

Five points were measured before each etch, the films were etched, then the same five points (to within a few millimeters) were measured again. The average of the differences of these five points, divided by the etch time, determined the etch rates.

Opaque Films (single-crystal silicon, metals) were patterned with photoresist. In some cases, the photoresist was left on the wafers for the etch. In others, as appropriate, the material was patterned and the PR was removed before the etch test. The SCS was covered with patterned nitride for the hot KOH etch.

A step height near the center of the wafer was measured with the Alphastep, the film was etched, and then the same step (to within a few tenths of a millimeter) was measured again. The step height difference and the etch rate of the photoresist or substrate then determined the etch rate of the film.

Plasma Etching

Plasma etching was done for one-half or one minute with one wafer in the etch chamber. Care was tak n to avoid plasma-hardening effects with the photoresist samples.

Plasma etch rates on patterned wafers can be quite different from those listed here for two reasons:

1. Some plasma etch rates tend to increase when there is less surface area to be etched, due to higher etch gas concentrations.
2. Usually be etched under those conditions (e.g., oxide in the poly etcher, LAM 1). These wafers were etched alone so that no etch gas was consumed by the normally etched material.

Wet Etching

Faster wet etches were done for one minute (even less for a few very rapid etches). All slower wet etches were done for at least 10 minutes to get a more accurate measurement.

Accuracy

For etches in which the computed standard deviation was smaller than the average rate, that etch rate is listed. In cases where the standard deviation was larger than the average (or the surfaces were very rough when Alphastep measurements were used), an upper limit is given (i.e. < 50). Etch rates of zero are given where the films were thicker after the etch, as often happened with photoresist in wet etches. In a few cases, the entire film was etched off in a short time; a lower limit is listed for these etch rates. My measurements are rounded to two significant figures. I estimate my results to be good to within ± 10% ± 5 A/min.

Final N tes

Because etch rates will vary with surface area exposed, cleanliness of chamber, other materials present, ag and previous use of solution, temperature of solution, temperature of chamber, other variables, and seemingly, phase of the moon, do not expect your results to be the same as those listed here! I have therefore included etch rates that other lab users and I have observed for many of the etchant/material

combinations to give an idea of how much etch rates can vary. Note that the top rows (all my own observations) are with fresh solutions and recently cleaned chambers, while the "Observed Range" high and low can b for older solutions, etc.

Sample Preparation

Most of the materials listed here are commonly used in the Microlab; others have been included for comparison. Three different popular KTI photoresist hardbake times were used to determine the effect of longer bake times.

SC Si <100>
Single Crystal Silicon with <100> orientation.

Poly n+
In-situ heavily n-doped polycrystalline silicon. RI = 3.97.
Deposited on a wafer with thermal oxide already on it to enable thickness measurements.
Deposited in Tylan 11 using recipe SDOPOLYG: SiH_4 = 120 sccm, PH_3 = 1 sccm, 650°C.
No anneal.

Wet Ox
Silicon dioxide grown in water vapor. RI = 1.46.
Grown in Tylan 2 using program SWETOXB: grown at 1100°C, p = 1 atm, with a 20 minute N_2 anneal at 1100°C.

Dry Ox
Silicon dioxide grown in dry oxygen. RI = 1.46.
Grown in Tylan 2 using program SDRYOXB: grown at 1100°C, p = 1 atm, with a 30 minute N_2 ann al at 1100°C.

LTO Undop
Undoped, annealed low temperature oxide. RI = 1.46.
Deposited in Tylan 12 using recipe VDOLTOC: SiH_4 = 60 sccm, O_2 = 90 sccm, PH_3 = 0 sccm (no doping), 450°C, p = 300 mT.
Annealed in N_2 in Tylan 2 using program N2 ANNEAL at 1000°C for 60 minutes.

PSG Unanl
High-doped phosphosilicate glass with no anneal. RI = 1.47.
Deposited in Tylan 12 using recipe VDOLTOC: SiH_4 = 60 sccm, Od = 90 sccm, PH_3 = 10.3 sccm (high doping), T = 450°C, p =300 mT.

PSG Hidop
High-doped, annealed phosphosilicate glass. RI = 1.48.
Deposited in Tylan 12 using recipe VDOLTOC: SiH_4 = 60 sccm, O_2 = 90 sccm, PH_3 = 10.3 sccm (high doping), T = 450°C, p = 300 mT.
Annealed in N_2 in Tylan 2 using program N2ANNEAL at 1000°C for 60 minutes.

Stoch Nitrid
Stochiometric silicon nitride (Si3N4). RI = 1.99.
Deposited in Tylan 9 using program SNITD: NH3 = 75 sccm, SiH_2Cl_2 = 25 sccm, p = 200 mT, T = 800°C.

Low-σnitrid
Low-stress silicon nitride (silicon-rich Si_xN_y).RI = 2.18.
Deposited in Tylan 9 using program SNITD.V : NH_3 =16 sccm, SiH_2Cl_2 = 64 sccm, p = 300 mT, T = 835°C.

Al/2% Si
Sputtered aluminum with 2% silicon in the target.
Deposited in the CPA at P = 4.5 kW, track speed = 20 cm/min, p = 6 mT.

Sput Tung

Sputtered tungsten.
Deposited in the CPA at P = 4.5 kW, track speed = 10 cm/min, p = 6 mT.
(Most of my tungsten peeled off my wafers due to residual stress. P = 2.9 - 3.1 kW should reduce this problem.)

Sput Ti
Sputtered titanium.
Deposited in the CPA at P = 4.5 kW, track speed = 10 cm/min, p = 6 mT.

Sput Ti/W
Sputtered 90% titanium/10% tungsten alloy.
Deposited at Stanford; conditions unknown.
Used as an adhesion layer for tungsten.

KTI 20 mn
OCG 825 (G-line) photoresist hardbaked 20 minutes at 120°C. RI = 1.63.
Deposited using Eaton program 10.

KTI 1 hr
OCG 825 (G-line) photoresist hardbaked 1 hour at 120°C. RI = 1.65.
Deposited using Eaton program 10.

KTI 1 dy
OCG 825 (G-line) photoresist hardbaked 1 day at 120°C. RI = 1.67.
Deposited using Eaton program 10.

Olin Hunt
Olin Hunt 6512 (I-line) photoresist hardbaked 30 minutes. RI = 1.63.
Deposited using Eaton program 15.

Etchants and Tips on their Use

All etches were done at room temperature (about 20°C) unless otherwise indicated.
All wet etches were done with fresh solutions, agitating occasionally.
All plasma etches were done with recently cleaned chambers.

Conc. HF (49%)
Concentrated hydrofluoric acid (49% by weight).

From bottle.
Etches oxides very rapidly. Often used to remove sacrificial PSG when micromachining.

10:1 HF

1 : 10 HF : H_2O (HF from bottl).
Typically used for stripping oxide and HF dips.

25:1 HF

1:25 HF: H_2O (HF from bottle).
Used for HF dips to strip native oxide without removing much of other oxides on the wafer.

5:1 BHF

5 : 1 buffered hydrofluoric acid (a.k.a. buffered oxide etch, BOE).
From bottle.
Pattern with photoresist.
Because this solution is buffered, its etch rate does not vary much with use. Best for controlled etching of oxides.

Silicon Etchant – Polycrystalline Silicon (Bell Labs)

This solution is mixed and bottled by Microlab staff. Bottles are stored in the tall white acid cabinet next to sink 432C (old lab).
Etch rate ~ 100 Å/sec
33% DI water / 3% NH_4F / 64% HNO_3
Bottle content:
960 ml DI water
75 ml NH_4F
1890 ml HNO_3

Phos. Acid 160°C

Phosphoric acid (85% by weight) at 160°C.
From bottle.
Heated at designated bath in Sink 7.
Used for wet etching of nitride. The nitride is typically patterned with densified low-doped PSG (densifying at 1000°C for an hour will not affect low-stress nitride).
If the PSG mask is not densified, it will be removed faster and may also have microcracks through which the acid can seep.
The nitride can also be patterned with poly.
Etch rate varies significantly with temperature.
The rate (in A/min, T in °C (!)) fits the equation 0.0872exp[0.0386T].

KOH 80°C

Potassium hydroxide solution at 80°C.
Mixed from 1000 g KOH pellets : 2 liters H_2O.
Heated at right side of Sink 3.
Solution is self heating. Let it sit a few hours before using.
Pattern with nitride.
Used for anisotropic etching of single-crystal silicon.
Attacks (100) and (110) planes much faster than (111) planes.
Etch rates listed here are down in the <100> direction.

Al Etchant

Aluminum etchant Type A from bottle at 50°C.
This solution is sold commercially and is supposed to etch aluminum at 6000 A/min. It contains phosphoric and acetic acids, but their concentrations are unknown.
Heated at designated bath at Sink 8.
Used for wet etching of aluminum.Etch rate decreases significantly with use.

Ti Etchant #2

Second titanium etch solution listed in the lab manual.

Mixed from 20 : 1 : 1 H_2O : HF : H_2O_2.
Titanium wet etch. Due to HF content, it also etches oxides.
Pattern with photoresist.

H_2O_2 30%

Concentrated hydrogen peroxide (30% by weight).
From bottle.
Used to wet etch tungsten and its alloys, which can be patterned O_2 with photoresist.

Piranha 120°C

Piranha solution at Sink 8.
This consists of about 5.6 liters of H_2SO_4 held at 120°C to which 100 ml of H_2O_2 is added immediately before use.
Used to clean wafers. Strips photoresist and metals, while not affecting silicon, oxides, and nitrides.

Acetone

Acetone spray strip using MTI program 10.
Used to strip photoresist.
While acetone readily stripped all the photoresists listed in this table, its effectiveness depends on the processing the PR has gone through. Heating the PR by a few tens of degrees above 120°C, eith r while hardbaking or during a process step, will make it significantly harder. Some plasma processing will have a similar effect (known as "plasma hardening"). In such cases, an oxygen plasma can be used to remove the PR.

Tech-c O_2 50 W

Technics-c plasma, O_2 = 51.1 sccm, 50 W.
One wafer.
Used for "descumming" freshly developed photoresist (typically for one minute).
Unbaked OCG 825 PR was removed at 330 A/min during a descum test.

Tech-c O_2 400 W

Technics-c plasma, O_2 = 51.1 sccm, 400 W.
One wafer.
This oxygen plasma is used to ash (strip) photoresist for 5 - 10 minutes. A power of 300 W for 7 min is also often used. It has been argued that the lower power is better because less plasma hardening occurs stripping. The Technics-c can hold up to four 4-inch wafers. A loading effect, in which the etch rate decreases when there is more to etch, is seen. In a 400 W PR stripping test, ashing four wafers at the same time was 23% slower than one alone.

Tech-c SF_6+He 100 W

Technics-c plasma, SF_6 = 12.9 sccm, He = 21.0 sccm, 100 W.
One wafer.
Used to plasma etch nitride. Unfortunately, it removes poly isotropically at about the same rate.
Pattern with photoresist.
This etch exhibits a severe loading effect. It is not only affected by the number of wafers in the chamber, but also by the fraction of surface area of nitride exposed. Furthermore, the etch rate varies with position in the chamber, so wafers should be rotated 3-4 times during an etch (some users also move their wafers among the four positions in a "planetary" motion).
Plasma etching, especially at higher power, heats the chamber, which may affect etch rates and thus selectivity. During all Technics-c tests, the plate temperature varied from 20 to 30°C.

Tech-c Freons+He 200 W

Technics-c plasma, CF_4 (Freon 14) = 10.0 sccm, CHF_3 (Freon 23) = 5.0 sccm, He = 10.0 sccm, 200 W. One wafer.
Another nitride plasma etch. Same gases as LAM 2 uses.

LAM 1 300 W

LAM 1 plasma, standard recipe: CCl4 = 130 sccm, O_2 = 15 sccm, He = 130 sccm, gap = 1.5 cm, p = 280 mT, P = 300 W.
Poly plasma etch.

Pattern with photoresist. If total etch times longer than about 2 minutes are required, break the etch up into several shorter times, giving the PR a chance to cool and thus erode less.

LAM 2 850 W

LAM 2 plasma, standard recipe: CF_4 = 90 sccm, CHF_3 = 30 sccm, He = 120 sccm, gap = 0.38 cm, p = 2.8 T, P = 850 W.
Oxide plasma etch.
Also etches nitride well, but such use is allowed by special permission only.
Pattern with photoresist.
If total etch times longer than about 2 minutes are required, break the etch up into several shorter times, giving the PR a chance to cool and thus erode less.

LAM 2 450 W

LAM 2 plasma, standard recipe, but lower power: CF_4 = 90 sccm, CHF_3 = 30 sccm, He = 120 sccm, gap = 0.38 cm, p = 2.8 T, P = 450 W.
Some users have had better results using this lower power.

LAM 3 Al Recipe

LAM 3 plasma, standard recipe: BCl_3 = 50 sccm, N_2 = 50 sccm, Cl_2 = 30 sccm, $CHCl_3$ = 20 sccm, p = 250 mT, P = 250 W.
All etches followed by airlock processing: CF_4 = 90 sccm, O_2 = 10 sccm, P = 400 W, for 1 minute.
Aluminum plasma etch. For thick layers of Al, either thicker photoresist or especially hardened PR must be used (use the hardening process known as "PRIST"). The airlock recipe, necessary to remove chorine from the wafers, is not supposed to do any etching.

LAM 3 W Recipe

LAM 3 plasma, tungsten recipe: SF6 = 20 sccm, p = 100 mT, P = 125 W. No airlock processing.
Tungsten plasma etch.
Attacks poly isotropically.
By special permission only.
This process may be replaced a tungsten etch in the Tegal etcher.

Tegal

Tegal plasma etcher is not ready for use at this date.
It will be used for etching both nitride and tungsten.

K. Williams
12/96
Rev.
11/97

THE PATENT & TRADEMARK OFFICE MAILROOM DATE STAMPED HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS DATE THE PATENT & TRADEMARK OFFICE RECEIVED:

Supplemental Information Disclosure Statement (3 pages); and Form PTO/SB/08 (1 page) with attached references.

Invention:	ETCHANT WITH SELECTIVITY FOR DOPED SILICON DIOXIDE OVER UNDOPED SILICON DIOXIDE AND SILICON NITRIDE, PROCESSES WHICH EMPLOY THE ETCHANT, AND STRUCTURES FORMED THEREBY
Applicant(s):	Ko et al.
Filing Date:	November 13, 2000
Serial No.:	09/711,324
Date Sent:	September 4, 2003 via first class mail
Docket No.:	2269-3526.4US
BGP/dlm:djp	

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Ko et al.

Serial No.: 09/711,324

Filed: November 13, 2000

For: ETCHANT WITH SELECTIVITY FOR DOPED SILICON DIOXIDE OVER UNDOPED SILICON DIOXIDE AND SILICON NITRIDE, PROCESSES WHICH EMPLOY THE ETCHANT, AND STRUCTURES FORMED THEREBY

Confirmation No.: 7008

Examiner: K. Chen

Group Art Unit: 1765

Attorney Docket No.: 2269-3526.4US
(97-1136.05/US)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

September 4, 2003
Date

Signature

Deidra Pfeil
Name (Type/Print)

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 be considered by the Examiner and made of record. Copies of the listed documents are enclosed pursuant to 37 C.F.R.

§ 1.98(a). The listed documents were cited by the Office in co-pending application Serial No. 09/610,049, filed on July 5, 2000, and directed to a related invention.

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

U.S. Patent No.	Publication Date	Patentee
US - 5,202,849	04/1993	Nozaki
US - 5,648,175	07/1997	Russell et al.
US - 5,948,701	09/1999	Chooi et al.

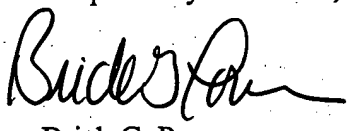
Applicants offer to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed after the mailing date of the first Office Action on the merits.

I hereby certify that no item of information contained in the Supplemental Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable

inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of the statement, and therefore no fee is due.

Respectfully submitted,



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Date: September 4, 2003
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	09/711,324
Filing Date	November 13, 2000
First Named Inventor	Ko et al.
Group Art Unit	1765
Examiner Name	K. Chen
Attorney Docket Number	2269-3526.4US (97-1136.05/US)

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.[1]	Document Number: Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-5,202,849	04/1993	Nozaki	
		US- 5,648,175	07/1997	Russell et al.	
		US- 5,948,701	09/1999	Chooi et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] - Number[4] - Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

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